JPRS-EST-90-014
13 JUNE 1990


# JPRS Report



# Science & Technology

## Europe

## SIXTH MICROCOMPUTER, MICROPROCESSOR APPLICATIONS SYSTEM

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13 JUNE 1990

# SCIENCE & TECHNOLOGY

## EUROPE

## SIXTH MICROCOMPUTER, MICROPROCESSOR APPLICATIONS SYMPOSIUM

36980026 Budapest SIXTH SYMPOSIUM ON MICROCOMPUTER AND MICROPROCESSOR APPLICATIONS in English 17-19 Oct 89

[Selected papers from the Sixth Sumposium on Microcomputer and Microprocessor Applications, held 17-19 Oct 89 in Budapest, sponsored by the IEEE Hungary Section, State Office of Technical Development, Hungarian Academy of Sciences, Ministry of Industry, and the Computer Research and Innovation Center]

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# COMBINED 2D AND 3D ROBOT VISION SYSTEM

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One of the most important challenges in machine vision is 3D data acquisition and processing. Acquisition speed is a major limitation of 3D sensing devices. An accurate and fast 3D range finder is presented which works on the new double synchronized scanning principle and produces a distance image in less then 1 second. A new method is proposed for the combined evaluation of intensity and range data based on the physical properties of the structured laser light illumination.

## INTRODUCTION

The automation of assembly and handling of tools or workpieces can be performed by the integration of sensory systems only. Sensors have a fundamental importance in this process. Sensors used in manufacturing systems can be classified in two groups:

- Obtaining internal data from robots (e.g. joint position, angular velocity, etc.)
- Obtaining external data from the environment to detect the presence, type, orientation, surface or other characteristics of objects in order to perform different operations with them.

The majority of robots installed in industry until now are used in less complicated working processes. The control of the necessary robot movements in these simple cases are usually performed without external sensors. Handling of tools and workpieces without any control or supervision is possible only with significant increase of costs due to the employment of additional accessories, for example, in the form of precision made conveyors. Though such a complicated and rather expensive investement eliminates the problem of sophisticated robot sensor systems, it has a negative effect on production, viz., neither complex manufacturing tasks nor flexible production can be accomplished.

The solution to this problem is to use an adequate sensory system which supplies precise information from the environment to the robot controller. Such a system is difficult to imagine without image processing unit. Early vision systems were designed on the basis of intensity sensing. Various methods

have been developed to evaluate such pictures to recognise objects. Intensity picture however depends on the effects of environment, they are difficult to evaluate and also the volumetric properties are suppressed. On the other hand, object recognition is not the only task to be solved in robot vision. One needs to measure position, orientation and distances for adequate robot control. For these purpose range sensing techniques offer a practical solution. The more is the complexity of the sensor system, better is the information achieved. The application of combined 2D (intensity) and 3D (range) sensors seems to be a good choice to solve these sensing problems.

## SENSORS FOR THREE DIMENSIONAL VISION

In general, vision systems are composed of an illuminating wave and detector system. 3-D systems can be classified as active or passive ones depending on the application of the illuminating wave.

In passive systems the illumination is independent on the measuring system (ambient illumination). Passive techniques are much more flexible than the active techniques. However, the passive approaches generally place a large burden on post-detection processing of the data.

The most obvious passive system based on the triangulation theorem is the comparison of stereo pairs, i.e., images taken from opposite ends of a known baseline by two cameras situated in a strictly defined geometrical arrangement. The main problem is locating matching points. One way of simplifying this task is to precede the matching algorithm by an edge detection algorithm to reduce the number of points involved. This is particularly useful for scenes of simple geometric objects. Another means of reducing the required computation is to use a hierarchical approach that first matches images at very coarse resolution and then proceeds to matches at progressively finer resolution scales. This is particularly useful where global matches are desired but might ordinarly be difficult to obtain due to lighting or geometric distortion variations that change over the scene. Considering the big amount of picture data and the present technological level we come to the conclusion that such a system cannot be used in industry yet.

Active techniques eliminate the correspondance problem and measure the depth directly by using a beam of energy and recording the time of flight (sonar, radar applications), displacement (structured light triangulation and grid coding), phase shift of a laser beam compared to a reference ( laser radar), or shadow length (directional illumination). Extensive post-detection processing of data for a depth map is avoided.

As small distances increase problems in connection with the measurement of the time of flight and phase shift, triangulation offers the greatest potential for acquiring a dense, high depth resolution 3D image at nearly video data rates and at low cost.

There are several systems where structured light is employed: punctual (with deflection), split beam, raster blend, etc. The use of more complex arrangement of light sources makes the post-detection algorithm more complicated. On the other hand the number of necessary measurements can be reduced when calculating a distance image. Uniqueness is guaranteed only in the case of punctual projection. Consequently this solution offers the simplest construction and fastest data acquisition time.

## LASER SCANNER BASED ON THE DOUBLE SYNCHRONIZATION

At the Technical University of Budapest in cooperation with the University of Karlsruhe (FRG) we are developing a triangulation laser scanner for combined evaluation of

intensity and range data. The system works on a new scanning method called double synchronization.

Figure 1. illustrates the principle of triangulation. Light beam comes from a laser source. The reflected signal is detected by a sensor (a position sensitive diode or a CCD line in our case) situated at a distance of d (baseline). The source, the reflection point of the object (P) and the sensor form a triangle. Knowing the side lengths or the angles of this triangle the distance between any object point and the source of the laser beam or the origin of the coordinate system can be determined.

The source of the laser beam is situated in the origin of the coordinate system (x,y,z). The object point P is projected to the B pixel of the picture plane (x',y' coordinate system) which is at a distance of f (focal length) from the detector model. Distance data can be calculated if we know either the horizontal or the vertical deviation angle of the emitted beam and the calibration parameters d and f by measuring both the pixel coordinates x' and y'. In this case, x' and y' values correspond to the horizontal and vertical deviation angle respectively.

If we use a parallel projection instead of the central one, and calculate the distance of the object point P' from the base line (h) instead that of P (fig.2), two angles out of the four (e.g. $\beta$ and $\gamma$) are sufficient to determine h. The parallel projection is advantegeous in volumetric calculations (centre of gravity, mass) and 3D representation as well. From fig.2 distance h can be written in the following form:

$$h = \frac{d}{\cot \gamma + x/f_0}$$

The main parts of a laser scanner based 3D vision system are the laser source, the deflection unit and the detector part.

The laser source must have an optical power large enough to produce a detectable light spot. However, for machine vision applications, it is desirable to use a low power laser because of cost and eye safety considerations. Due to the wide variation in surface quality the recived optical power is mostly not more than 0.001% of the laser power. On the other hand specular reflection directed toward the detector will produce a signal level which is higher in several orders of magnitude. Variation of surface quality in the area of the light-spot causes an error by the spot position detection, i.e. small spot diameter is needed.

An advanced detection method for light-spot position makes use of position sensitive detector called a lateral effect photodiode. The continous position detectors locate the centroid of the light spot making them somewhat insensitive to focusing. The signal-to-noise ratio is directly proportional to the amount of light received. Therfore one must be aware of decreasing performance when viewing dark surfaces. On the other hand specular reflection causes an overflow of the detector. Position values on this places are not evaluable.

If we use a CCD array instead of the PSD, the dynamic range of the detectable light can be increased. The inherent property of CCD's, namely the integration of incident light energy increases performance where poore reflection occures, and an advanced blooming compensator makes the detection of very high light intensity possible. However, the use of the CCD's generally places a large hurden on speed of the detection if we use a 2D array. Linear array techniques are faster, and they are the most widely used detectors in profile scanners, but they are not directly available for 2D scanners.

A large number of methods exist for deflection of the laser light. Solid state acusto-optic cells, polygon mirrors, resonant scanners or holographic devices offer capability for scanning at high rates. For our purposes of industrial sensing

a random scanner is needed and therefore we use galvano-mirrors in our system.

Fig.3 shows the structure of a basic triangulation scanner schematically. The beam of a laser is directed towards the galvano-mirrors. The reflected light is measured by a PSD or a 2D CCD array. The bottleneck of performance in this case is the overlapping of variation in light spot position due to the deflection and depth change. Therefore one need to use a large baseline size for appropriate range resolution which has a negative effect on the shadowing problem.

A popular technique is synchronized laser scanning. This method, which is equivalent to tracking of the scanning light spot, has several advantages which include reduction of the baseline size without compromising resolution, ability to use a small high speed detector, reduction of shadowing, and improved rejection of ambient light. Each of these advantages become very important in industrial applications where implementation of the triangulation method would otherwise be cumbersome. Synchronized scanning can be used in either electro-mechanical or solid state scanning systems.

Fig.4 shows the structure of the synchronized profile scanner proposed by Rioux. The laser light is reflected (and deflected) on the first face of the galvano-mirror. The reflected light falls through a fixed mirror on the backside of the same galvano-mirror. This method of tracking is robust, cost-effective and easy to implement for profile scanning.

There are some implementation of the technique explained above for 2D scanning. A popular method is the use of cylindrical lenses for reducing the picture size perpendicular to the direction of syncronization. In this case one need to use two dimensional detector (PSD or 2D CCD array) because of the limited ratio of the focal length belonging to the main optical axes of the objective with cylindrical lenses. Another possibility is the integration of a third galvano-mirror for tracking the laser-spot in the nonsynchronized direction. This method offers the integration of linear detectors. However the control of this mirror combined with a random deflection is complicated and therefore it becomes the limiting factor in the data acqusition speed.

Fig.5 shows the structure of our 2D synchronized scanner based on the extension of the method of Rioux for two dimension.

The beam of a 20 mW diode laser is directed towards a galvano-mirror with two separated region. The laser beam is deflected on one of these regions in the vertical direction (perpendicular to the baseline), and is directed towards the mirror for horizontal deflection. The beam, deflected in both direction is emitted by use of a fixed mirror.

The detected light is synchronized based on Rioux's method with the opposite side of the horizontal mirror. The horizontal synchronized beam is deflected with the second region of the vertical mirror. On this stage the position of the laser-spot is nearly independent from the deflection angles. Variation in the distance relative to the geometrical center of the system causes the variation of this position. However this change appears in the horizontal direction only. On that reason we can use linear CCD detector with simple optics.

The speed of the system depends on the number of pixels in the distance image, the amount of incident light and the number of pixels in the shadow. The average exposure time for a $256^2$ image is in the order of few seconds. The resolution is a result of a compromise. The mathematical analysis of the geometry is out of scope of this paper, but obviously, high performance range resolution reduces the depth of view. The resolution using our system was designed to be 0.2mm for an object distance of 1500mm, for a depth of view of 200mm and with an equivalent baseline length of 300mm.

The signal of the CCD detector is evaluated by hardware. It produces a blooming-compensated position value. The intensity of the reflected light is measured by use of a

photodetector mounted separately. The signal of this detector is quantised and stored for each pixel in the distance image. A commonly used CCD camera is placed in the middle of the optical axis of the system. Its task is to pickup a passive intensity picture for extended evaluation of shadow areas. The laser scanner is controlled by a processor system based on the microprocessor Motorola 68000. Its task is the control of the deflection, the calculation of the range values and the compensation of distortions (e.g. parallax, pin-cushion distortion, etc.). The geometrical constans of the system are determined through a selfcalibration procedure by use of reference planes.

Fig.5 and 6 shows the distance and intensity image of a coffee cup respectively.

## COMBINED EVALUATION OF INTENSITY AND RANGE DATA

There are three different kinds of data produced by the laser scanner:

- Normal range data corrected on the basis of the local intensity (values over the noise limit)
- Pixels belonging to shadow-areas
- Background data

Pixels belonging to shadows or background are marked in the range matrix.

Due to the large variation of surface quality and to the distortion of the laser-spot geometry on volumetric contours of objects the range data of them are mostly not considerable. The segmentation of volumetric surface regions based on range data is very time-consumptive. On the other hand both of textural and volumetric contours produce fast intensity changes. These intensity variations are easy to detect, therefore the position of contours is defined on the basis of the intensity data rather then the range data in our system. Textural and volumetric contours can be separated with the analysis of the range data on a strip along this contours. The volumetric contours divide the scene into elementary regions. The characteristics of surface segments are defined by the use of range data at very high speed.

As shadow areas are without ambiguity marked in the range matrix, it is possible (due to the random scan capability of the scanner) to drive the laser beam along the boundary of the shadow area. The laser light causes a saturation in the passive intensity picture. There are the shadow regions of the laser scanner marked in the CCD camera picture exposed in this case. The evaluation of these regions in the camera picture makes the correction of range data and the solving of ambiguity problems on the recognition level possible.

The scanning method is very sensitive for textural variations which makes a surface quality control possible with the same sensor system.

## CONCLUSIONS

Structured light methods seem to be a promising approach to 3D vision. The double synchronized laser scanner provides accurate and fast range data acquisition for industrial application. The combined evaluation of intensity and range data seems to be useful aiming to extract volumetric properties at very high speed. On the basis of the special sensitivity for textural variations the system is predestinated for quality control tasks.

A new system is under development based on these experiences. The scanner-system will work on the same

principle. A special hardware processor will provide the combined evaluation with an increased speed. The system will be in operation in 1990.

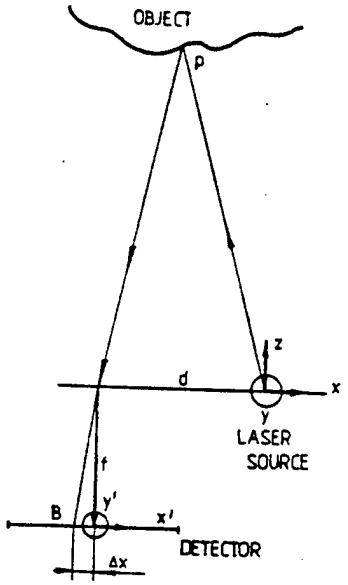



FIG.1.

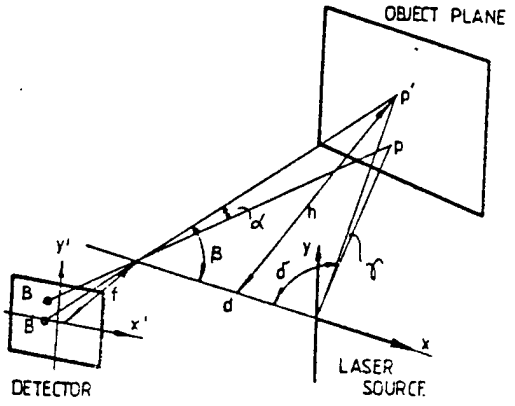
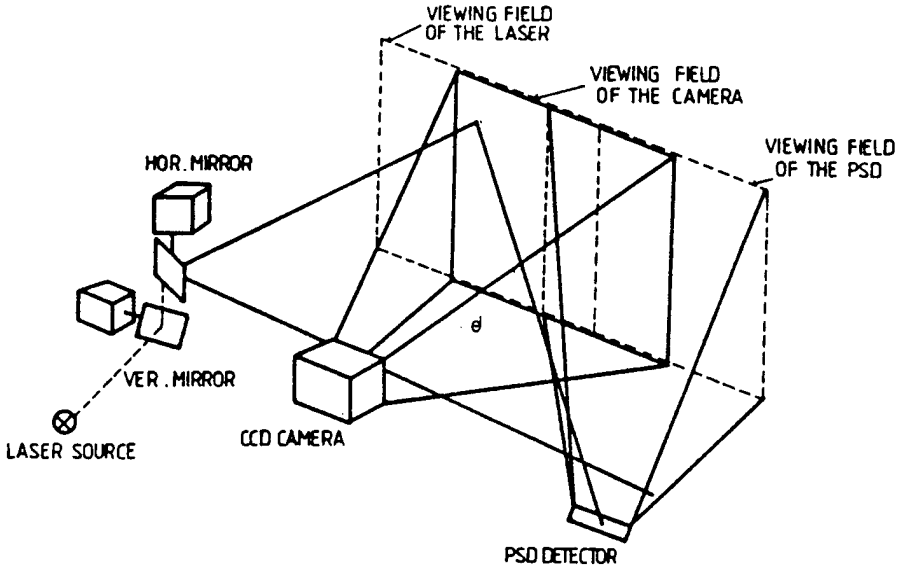



FIG.2.


VIEWING FIELD
OF THE LASER
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OF THE CAMERA
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VER. MIRROR
LASER SOURCE
CCD CAMERA
PSD DETECTOR

FIG.3.

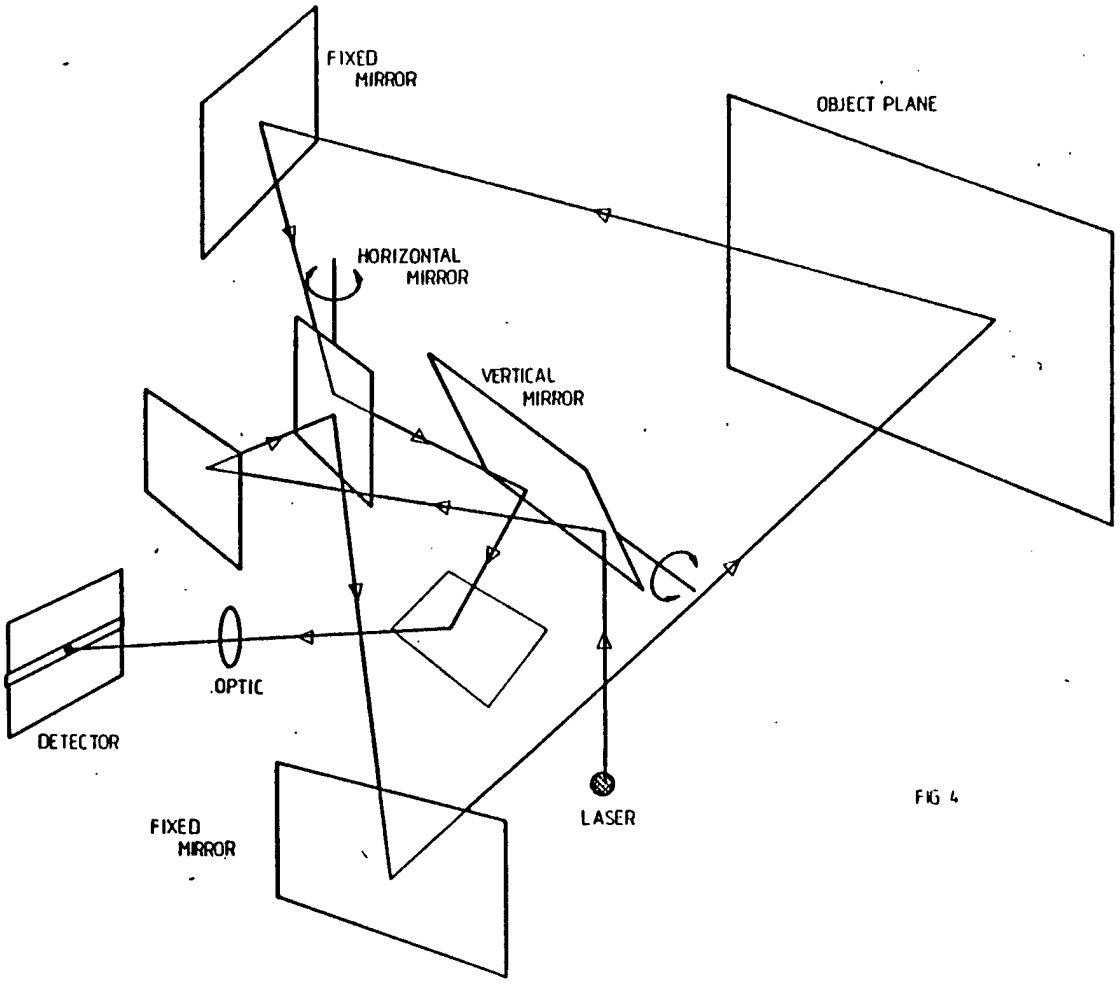
FIXED
MIRROR
OBJECT PLANE
HORIZONTAL
MIRROR
VERTICAL
MIRROR
OPTIC
DETECTOR
FIXED
MIRROR
LASER

FIG 4

FIG.5.

FIG.6.

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# INTLAN - A Novell compatible INTegrated service Local Area Network

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INTLAN is an integrated service local area network which allows PC-based integrated workstations to communicate with each other by simultaneous voice and data connections. The paper describes the motivation of the project, the technical specifications of the network and the structure of the applied INTLAN controller board.

## MOTIVATIONS AND THE INTENDED APPLICATION AREA

The traditional solution of integrating voice and data in a local environment is based on the company's existing local telephone exchange and wiring. In this case, along with the usual voice communication services, data communication can be accomplished by means of modems. The data communication is based on the same circuit-switching technique.

The disadvantages are:

- only low communication speed is possible
- a line can be used for one type of functions only (either for voice or data) at a time.

Therefore implementing true integrated services is a difficult task. ISDN seems to solve the latter problem, but the 64kbps data rate, available at the basic subsciber interface, is by far not enough to support high-speed, bursty data communication demands.

Our approach seems to be a cost-effective offer for a modern office, where there is a demand for true integration of real-time voice communication and data transfer between PC-based integrated workstations. The services are embedded into the commonly used Novell Netware environment. A highly efficient channel access protocol is implemented on a special INTLAN board along with all the voice input/output and control functions.
The system is primarily intended to be a good solution for a newly furnished small-to-medium size office with approx. 15-20 workstations, provided that no more than two external phone lines, one telex connection and one line for telefax are needed. In this case, it is not necessary to install a PABX, since this integrated LAN can offer all the advanced services of a modern PABX. The above mentioned external connections can be embedded into an existing PABX network, thus providing integrated services only for that part of the company where integrated services are really of vital importance.

**TECHNICAL SPECIFICATIONS**

The network operates at 1Mbps on an inexpensive 75 Ohm thin coaxial cable bus which is terminated at both ends (See Fig.1.). Workstations are connected to the cable (e.g.) via T-connectors and short cables (mainly following the physical layer specification of the ISO 802.4 standard). Neither the maximum number of stations nor their placement along the cable are strictly limited by physical constraints. (However, the efficiency of the medium access protocol limits the number of stations.) Broadband signaling, CPFSK modulation is used (again, according to the above standard).

Any IBM PC XT/AT and compatible machines can be used as a workstation. For this purpose, an INTLAN controller board must be plugged into an empty extension slot of the PC and a specific driver for the Novell Netware software must be loaded which uses the INTLAN controller board for physical and data link layer control instead of, say, an ARCNET board. The voice i/o device (e.g. phone handset) is connected to the INTLAN board.
A PC-based hardware is dedicated to be the LAN-WAN gateway. The hardware contains special interface cards for external phone (telefax) and telex lines, and an INTLAN board.
A central timer unit must be attached to one end of the bus. This is a relatively simple hardware, generating timing information for the proper operation of the network at medium access level. It can be built in into the gateway unit.

## THE INTLAN CONTROLLER BOARD

The functions of the INTLAN card can be divided into two groups:

- phone control, i.e.:
  - voice interface functions (digitalization, silence detection, tone generation, handling of dialing pulses, e.t.c.)
  - call handling
  - special (PABX) functions (call redirection, call filtering, caller identification, e.t.c.)
- line control, i.e.:
  - interfacing to the cable (modem)
  - medium access control
  - data encapsulation/decapsulation
  - message buffering

It seemed to be obvious, that the two groups of functions should be controlled by two independent processors. The most simple solution for the PC-INTLAN interface can be a memory, mapped into the PC's address space. Consequently, the basic core of the INTLAN card is a multiport memory, which can be accessed from either the PC or the two INTLAN card processors (See Fig.2.).

ZILOG Z80 processor, AMI S3506 PCM codec, NEC uPD7201 Multiprotocol Serial Communication Controller, Philips NE5080-5081 modem chips and 8 K of common memory were used for the experimental system.

Framing signals of 30 msec are provided by the central timing unit. The messages are organized into HDLC-like packets and sent to the network by a new collision avoidance protocol (using implicit tokens). The voice packets can occupy not more than a certain percentage of the frame time (30msec), so a certain share can be granted to the data (Novell) packets. We use a simple (1:2 ratio) compressing algorithm for the internal calls, however, the external calls (through the gateway) will use the whole 64kbps voice channel. For example, if we allow 40% for the voice packets, there can be two external and two internal or six internal calls active in the same time.

The line control program can communicate with the phone control by using mailboxes in the common memory. The communication between the line control and the PC driver program is organized similarly, but one of the PC's interrupt lines is also used for signalling (See Fig.3.). The Novell Netware with the appropriate Novell-INTLAN driver will run on the PC. Some utility programs are also needed for aiding the user in using telex, telefax, (probably voice mail) and other services.

## CONCLUSIONS

The INTLAN integrates data and voice communication on the same network not only at the physical level (using the same

transmission medium) but also at the user level. As for the data communications, a user can run any application program under Novell Netware. Telephone conversations may be built up between any pair of stations, but a parallel voice connection can be established between workstations engaged in data communication, without any further calling procedure.

Using the LAN-WAN gateway unit, an INTLAN is connected to the public telephone and telex networks. Sending and receiving telex or telefax messages is accomplished by the gateway hardware and the Novell server machine. The voice quality - as far as the external calls are concerned - fully corresponds to the CCITT recommendations. In addition to the essential PABX functions, some value-added services are also available.

To the best of our knowledge, no commercially available LAN offers on-line voice communication capability and connection to the public network, meeting CCITT recommendations. Telex and telefax hardwares and softwares are available as separate products. However, our system comprises all the above functions into one network and offers them for the network users in a fully integrated way.

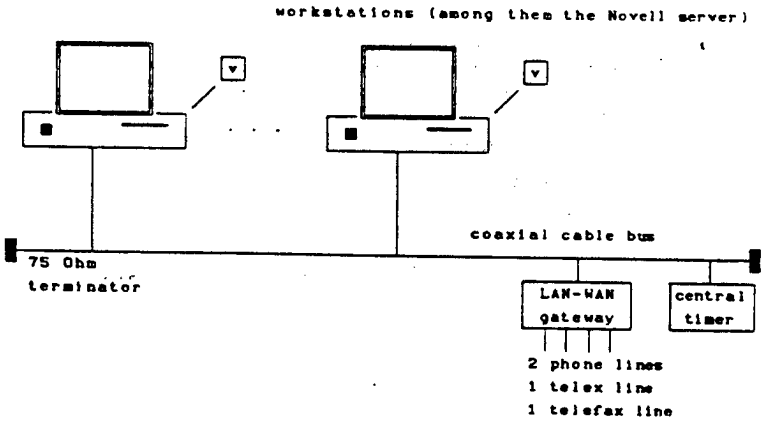



Fig.1. The topology of INTLAN

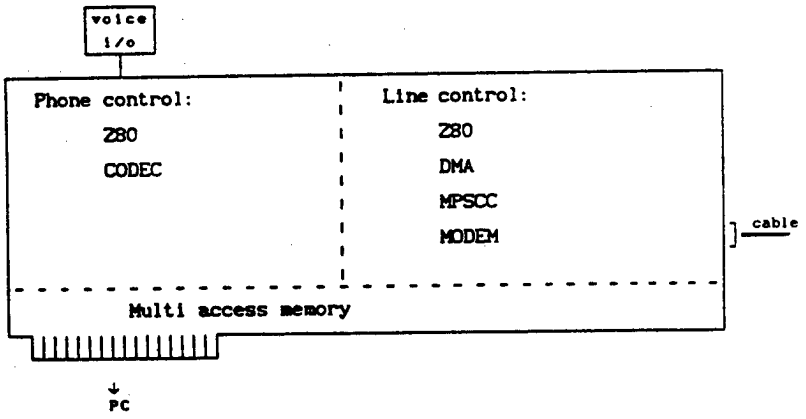
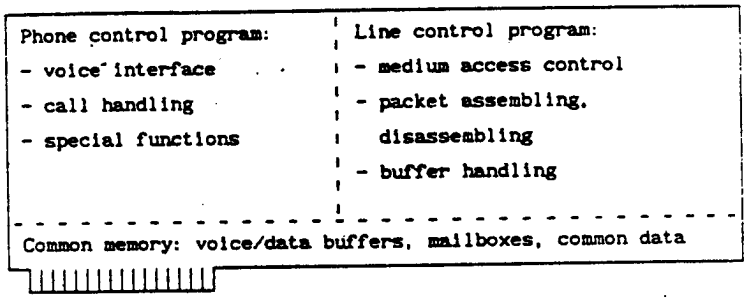



Fig.2. The INTLAN card hardware




PC: - Novell/INTLAN driver
- Novell (DOS)
- utilities

Fig.3. The INTLAN software

# Teletex System Implementation on Personal Computer

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In this paper a Teletex software development on a personal computer is described. The Teletex system requirements are standardized by Recommendations of CCITT. The modules of the software system, the parallel processes and the operation of the system will be discussed. Then the implementation of the session/document protocols and the application layer will be described. The language of the implementation is Modula-2.

## INTRODUCTION

The Hungarian Post decided to join the international Teletex service. Thus, the State Committee of Technical Development conducted a competition for developing a Teletex software/hardware system in Hungary. The Computer and Automation Institute of the Hungarian Academy of Sciences together with the TERTA have won the competition, and started research in 1987. The project, which includes the implementation of a prototype system, will probably be completed later this year. The main task is to develop an equipment which is rather cheap and meets the requirements of the international recommendations. In this paper the development of a Teletex system on a general purpose microcomputer is discussed. A brief overview on Teletex system's requirements is given in order to understand the implementation details.

## TELETEX SYSTEM'S REQUIREMENTS

Teletex is an international service enabling subscribers to exchange correspondence on an automatic memory to memory basis via telecommunication networks and it gives a high level user interface. Teletex service provides communication between terminals, which are used for the preparation, editing and printing of correspondence. The first Teletex equipment appeared in 1983 and about 30 countries in the world subscribed to the Teletex service up to 1987.

The basic requirements of Teletex services are as follows

- a basic level of compatibility of the terminals connected to the service. Terminals communicate character-coded information, the character repertoire is standardized
- automatic memory to memory transmission with transmission rate of minimum 2400 bit/sec
- local operation is not disrupted by incoming messages
- the content, the format and the layout of the messages sent and received should be identical
- worldwide compatibility with Telex terminals
- there is no restriction on the type of the used network
- the basic element of correspondence is the page. One or more pages form a document, which is considered an entity.

Taking into account the above requirements the Teletex service has been standardized between 1977 and 1980. The main fields of the standardization are general operational rules [1], terminal equipment capability [2], character repertoire [3], control procedures for session/document levels [4], network-independent basic transport service [5].

Teletex Recommendations are in close connections with the 7-layer OSI Reference Model. The Teletex transport layer corresponds to the OSI Recommendation X.224 transport protocol class 0. The Teletex session/document layer is a subset of the OSI 5th layer. The control procedures of the 6th and 7th layers have not been standardized.

Recommendation T.61 specifies the character repetoire and the coded character sets for the international Teletex service. The Teletex character repertoire consists of graphic characters and control functions. Both groups contain basic and optional elements.

Recommendation T.70 discusses the network independent basic transport service for telematic services.

Three kinds of networks are considered: Circuit Switched Public Data Network (CSPDN), Packet Switched Public Data Network (PSPDN) and Public Switched Telephone Network (PSTN).

The transport layer hides the differences between networks for the session layer.

Recommendation T.62 specifies control procedures for session and document layers. The session layer uses the services of the transport layer. Its main tasks are to establish and terminate a session connection, to change the source/sink relationship, to transfer data between two terminals.

The session user information conveys information for the document procedures. At session initiation the calling terminal is defined to be the source (sending) terminal. Although the receiving terminal may indicate that it requests control, only the current source terminal may send 'Command Session Change Control'. A session may be terminated by the calling terminal only. It may, however, be aborted by both terminals in case of error.

The document layer's main tasks are to control normal document transfer, to carry out negotiation of optional capabilities and to use error recovery procedures.

During the normal transfer of a document several data blocks may be used to transfer the content of a page. The 'Command Document Page Boundary' indicates a page boundary and a checkpoint for error recovery. The receiver acknowledges that it takes responsibility for that page. The next page can be sent before the arrival of the acknowledgement of the previous page. The acknowledgement window size, 3 by default, shows the number of pages that can be transferred before the arrival of an acknowledgement. If no error is detected, 'Command Document End' is used to indicate the end of the document. A document is transferred when the acknowledgement of every page, including the last one, has been arrived.

If standardized optional terminal capabilities are required for the transfer the negotiation concerning the optional

capabilities is carried out by start commands. 'Command Document Capability List' can also be used for this purpose.
Negotiation covers the graphic character repertoire and control function sets, the storage capability required at the remote terminal, the value of the inactivity timer.
Error recovery procedures allow repeated transmission of information in case errors are detected.
'Command Document Continue' indicates that the transmission of a document transmitted already partially, is to be continued.
'Command Document Discard' indicates an abnormal end of a document and that the receiver may delete the fragment of the text already received. 'Command Document Resynchronize' indicates the point of resynchronization, it ends the document abnormally.

## HARDWARE CONFIGURATION

The Figure 1 shows the scheme of the hardware configuration. Both LINE1-card and KONKOLY-card are developed at the Computer and Automation Institute. A LINE1-card establishes connections between the PC and the international network. A KONKOLY-card, on the other hand, establishes connections in a local network in which the adapter is a node. There is a special case of the general configurations. The 'dedicated terminal' works as an adapter as well as a local terminal.

## SOFTWARE SYSTEM

The Teletex software system has two main tasks, on one hand it should transmit documents to and from the adapter's storage and the international network - network software, on the other hand it should provide local facilities for the preparation, editing and printing of documents - local software.
Using the general hardware configuration above, the network software is actually contained in the adapter and the local software in the local terminals. Hence, the former is called the "adapter software", while the latter the "terminal software". Further the adapter software will be treated only.

## STRUCTURE OF THE ADAPTER SOFTWARE

Figure 2 shows the main parts of the adapter software system.

Documents are stored on the "document storage", located on the fixed disk. The document storage software provides facilities to

- create a document
- read or write a document from its beginning on, or continuously, or from a specified page on
- modify a document head, including the status information
- delete a document.

These facilities are used by other software components rather than the user.
Documents are organized into queues. Some of them are listed below

- queue of urgent documents to be sent
- queue of normal documents to be sent
- queue of documents posted in advance
- queue of documents to be printed.

Also, the adapter software handles the "mail-book", which records the source and target terminals of documents and other data. These pieces of information can be displayed on the screen and they can be printed as well. The mail-book provides the documentation of the incoming and outgoing mail for the users.

The "trace log", which contains data for debugging, is another collection of information about the work of the software system. System components can read and write the entities of the trace log. The information in the trace log is intended for software specialists rather than users.

The interface to the international network as well as that to the local network are realized by queues of "buffers". A buffer contains an information entity, which can be a protocol block or some other control or data information. Buffers are logically organized into queues. There are 4 types of queues from the point of view of their destination:

- queue of buffers containing requests (request-queue)
- queue of buffers released from and free for the request-queue (request-free queue)
- queue of buffers containing indications (indication-queue)
- indication-free queue.

There is one queue of each type according to each point of connection to the international network (Transport Service Access Point). Similarly, there is one queue of each type corresponding to each point of connection to the Local Area Network (LAN).

The buffers module provides facilities to acquire or release a TSAP or a LAN-line, to get or put a buffer into or from a specified queue of buffers, and to test the status of a line. A pointer is assigned to each buffers. In order to minimize the actual information transfer, the buffer pointers, rather than the buffers themselves, are moved from one queue to another. For brevity, however, we say that the buffers are moved.

The "automatic starting" module starts the transmission of a document if there is a document to be sent, and there is free TSAP and buffers.

The modules of the "session/document/application layers" handle the transmission and the reception of documents respecting to the description of the session and the document layers in Recommendation T.62 and the application layer that is not standardized. They will be discussed in detail later.

The "transport layer" carries out the functions as specified in Recommendation T.70. Buffers containing protocol blocks created by the document and session layers are sent to the international network by this module.

The "Command Interpreter" receives the user commands from terminals, interprets and answers them. Figure 3 shows some user commands.

The Teletex system considers the "LAN software" performing the physical data transfer between the terminals and the adapter as a NETBIOS emulator. Buffers containing user commands and the responses created by the Command Interpreter are communicated between the adapter and the terminals.

The "printing module" handles the documents to be printed, those being printed and those having been printed. It prepares a document for the "printer-driver", which actually prints the document.

The "scheduler" controls parallel processing performed by various processes.

The software system is written mainly in Modula-2, though the printer-driver is written in C-language and the transport protocol is implemented in CDL-2. It was easy to integrate these modules to the main part.

## PARALLEL PROGRAMMING AND PROCESSES

The operational scheme of the system can be seen on Figure 4. Squares denote data items and polygons denote processes. The LAN-software transmits buffers containing a user command from a terminal to the adapter's 'indication-queue'. Command Interpreter realizes that a user command has arrived and it reacts accordingly. For instance, if a document has arrived then Command Interpreter stores it on the document storage.

The corresponding buffers are appended at the end of the 'indication-free queue'.
When it is time to transmit the document, Automatic Starting starts modules of session/document/application layers (sender), which send the document. They first initiate connection with the addressee, then they ask for the document which is on the document storage. They put both protocol commands and data to the buffers into the 'request-queue' of a TSAP. The transport layer detects the request and transmits it to the network. The corresponding buffers are appended at the 'request-free queue'. Similarly, responses of the called terminal are placed into the buffers of 'indication-queue' by the transport layer. Modules of session/document/application layers read those buffers, interpret them and place them into the 'indication-free queue'. On receiving a document, the mechanism is similar, but the direction is just the contrary.
On printing a document, the Command Interpreter puts the document into the queue of documents to be printed. The Printing process takes a document from the queue, prepares it for the Printer-Driver and puts it into the print-buffers. Print-buffers are different from the normal buffers in the system. They are longer and there are only two of them. Printer-Driver prints the contents of the print-buffers sequentially.
Obviously the number of the necessary protocol programs is the same as the number of the TSAP's to the international network in the system, and, similarly, the number of necessary Command Interpreters and LAN-software is the same as the number of the connection points to the local network. They work in parallel in the system.

As the language of the implementation Modula-2 has been chosen because it is a high level programming language which is suitable to implement quasi parallel systems excellently. Quasi parallel means that a single processor (CPU) executes several processes. Modula-2 uses the concepts of Process, Newprocess and Transfer, [6].
In terms of Modula-2 a process is a parameterless procedure which is started in a special way. Every process requires private workspace to allocate its local variable. If a procedure is started as a process several times, then the program code is common and the data fields of the individual instances are separate. Using these basic elements of Modula-2, everybody can easily write a suitable Process Scheduler. We use a Real Time Kernel that contains concepts of Semaphore, Signal and Scheduler.
The system contains the following processes in terms of Modula-2: Document-sender, Document-receiver, Transport (both sender and receiver), Command-interpreter, LAN-software, Printing process, Printer-driver, Automatic Starting.

The producer/consumer situations occurring in the Teletex system can be seen on Figure 5.
The processes communicate via signals.

## IMPLEMENTATION OF SESSION/DOCUMENT PROTOCOLS

Modules of session/document/application layers consist of modules of session/document layers and modules of application layer. The operation of protocol automata for session/document layers are specified strictly by State Transition "Diagrams" and State Transition "Tables" in Recommendation T.62. They determine the new states of the automata with respect to the current state, the transition function and the input signal. Input signals can be reception of a protocol block, a service primitive or a signal of a timer. Output actions may be starting or stopping a timer or generation of a protocol block or a service primitive.

Recommendation T.62 contains for the calling terminal and the called terminal one State Transition Table both for session and document layers. There are about 30 states and 50 input signals. This means that there are about 1500 elementary

records in a State Transition Table. Each record contains four data items: timer action, protocol action, service primitive and final state, which make 6000 data items altogether. There are separate State Transition Diagrams for the session and the document layers.

According to the OSI 7-level reference model, each layer uses only the services of the lower layer via the service primitives. Protocol blocks are sent through the lower layers and they are 'wrapped in' according to the requirements of the lower layers. They are 'wrapped out' at the partner terminal according to the layers which they are sent through.

A Transport Data Block may contain session commands or session data. Session data also convey document commands or document data. Commands for the appropriate layer are the input signals of the automaton of that layer. Data are sent to the higher layer and are analysed there.
The situation is a bit different in case of the Teletex layers. The session layer communicates with the application layer directly and what is more, the transport layer also can communicate directly with the application layer.
The main tasks of the protocol implementation are the implementation of the protocol automaton, the analysis of the protocol blocks, the realization of the service primitives.

## IMPLEMENTATION OF THE PROTOCOL AUTOMATON

Fundamentally, there are two possible ways to implement a protocol automaton. The first is to build the features of the automaton into the program, the second is to describe the structure of the automaton as data and to interpret it during the execution. Both methods have advantages. The first one requires a relatively small amount of memory and yields a fast program, but it is almost impossible to modify it. The main advantage of the second method is that the program and the data are independent. Moreover, this implementation reflects the recommendation on a better way. The actual implementation is easy, especially with the tools, such as procedure types, provided by Modula-2.
If the elementary record of the State Transition Table contains a parameterless procedure as an output action and a number as a final state then the State Transition Table in Modula-2 can be seen on Figure 6.

We applied the latter method. In order to decrease the size of the automaton the following modifications were introduced. State Transition Tables are divided in the same way as the State Transition Diagrams (Figure 7). This division is justified because session input signals are invalid during the document phase and document input signals are invalid during the session phase. There are only a few exceptions, such as transport disconnect indication, etc. This method decreases the size because some parts of the tables are omitted and some others are identical (sending protocol, receiving protocol).

Masks indicate the input signals that are significant in the states. One mask belongs to each state. A mask is a BITSET in Modula-2, one bit belongs to each input signal.

The description of the protocol automaton consists of two parts. The catalogue, indexed by the state, contains the mask and the address of the first element belonging to that state in the State Transition Table. The Transition Table itself contains records consisting of a final state and an output action.

The evaluation of the state transition is performed in two steps. First, on the basis of the mask, it is determined whether the current input signal is valid in the current state, and its serial number is calculated, too. Then the index of the actual record in the Transition Table is determined and the state transition is evaluated.
Thus, the size of the two Transition Tables are decreased from the original 12,000 (2*6,000) data items to about 1,000 data

items. There are four automata with 10 states in each. The number of valid state transitions is less than 100. Consequently the size of one automaton is less than 10*4*100*2=240.

## ANALYSIS OF PROTOCOL BLOCKS

It is carried out by the input/output procedures. The structures of the protocol blocks are standardized in Recommendation T.62.
Commands, parameter groups and parameters have the same structure. They consist of an identifier, a length indicator, and a parameter field. The parameter field of a command or a parameter group consists of a sequence of one or more parameter groups or parameters. Figure 8 shows a structure of a protocol block. Although a recursive structure of parameter groups is allowed, but a thorough investigation of the session and document commands shows that there is no recursion in them. The input procedures read the content of a protocol block and check its structure and the values. The result is an input signal to the protocol automaton and the saving data in a system data field if necessary. The output procedures generate protocol blocks on the basis of the system data field.

## REALIZATION OF SERVICE PRIMITIVES

Service primitives are realized as procedures. They are the tools of the communication between the different layers. They may be an output action of an automaton or they may generate an input signal to the automaton. In the latter case the state transition is evaluated. For instance, the service primitive 'Session Connect Request' prepares data for the transport layer, assigns input signal 'SConReq' to the automaton and calls for the evaluation of the state transition. The output action is 'SendTCR'. Both input/output procedures and service primitives are procedures and not processes. They can be nested in each other.

## THE APPLICATION LAYER

We use the word 'layer' though it does not correspond exactly to the OSI 7th layer. Its control procedures are not standardized. It contains decisions which are not prescribed in any Recommendations. This layer is an application only from the point of view of OSI layers, it is not an application from the point of view of the Teletex system. It controls sending or receiving a document and communicates between document storage and the protocol automata. There are two processes in this level, namely, Document sender and Document receiver. Let's mention few problems in connection with the implementation.

First of all standardized option handling must be treated. These are capabilities of the terminal equipment (see later). It is necessary to know what standardized options a document uses. The capability of a terminal might be enhanced and thus its software must be modified accordingly. Thus, it is useful to separate data and program in this case, too.
For this reason we use the concept of capability-vector, which is an ARRAY OF BOOLEAN, to record the standardized options. A BOOLEAN variable belongs to each standardized optional value of every control function. For instance, the control function 'page format selection' has two values belonging to the basic Teletex services and 14 optional values. So 14 elements of the capability-vector are used to indicate the presence/absence of these capabilities. There are a system capability-vector which shows the presence of these capabilities in the system and a capability-vector belonging to each document. Negotiations

concerning the optional capabilities (commands CDCL and RDCL) are realized on the basis of these capability-vectors.

Another problem is the scheduling of document sending. The sender of the document is asked about the 'from-to' interval in which the document should be sent. It begins to send the document as soon as the 'from' time comes. If the 'to' time is near, the document is passed over to the queue of 'urgent' documents. Documents with parts already sent are sent first. Then the 'urgent' documents are sent and finally the normal documents are scheduled.

Documents which cannot be sent are handled in two different ways. If the cause of the error can be corrected only by the sender then an errorcode is set in the head of the document and it is taken out of the queue of documents to be sent. An example for this situation is the case when the code-extension or the mnemonic in the address is wrong. If there is a hope for recovery (if, for instance, the remote terminal is busy), the system will repeat sending the document several times.

## CONCLUSIONS

Modula-2 proved to be a good tool to implement the Teletex system because of its facilities for handling quasi parallel processes, procedure type variables and BITSETs.
The size of protocol automaton of the session/document layers was decreased to a great extent, so it was possible to implement data independent protocol automata in a personal computer.
The implementation is as portable as the Modula-2 environment. Unfortunately the speed of the system is rather low. It is acceptable only because the Teletex system is only a quasi real-time system. For actual real-time systems, some other approaches must be found.

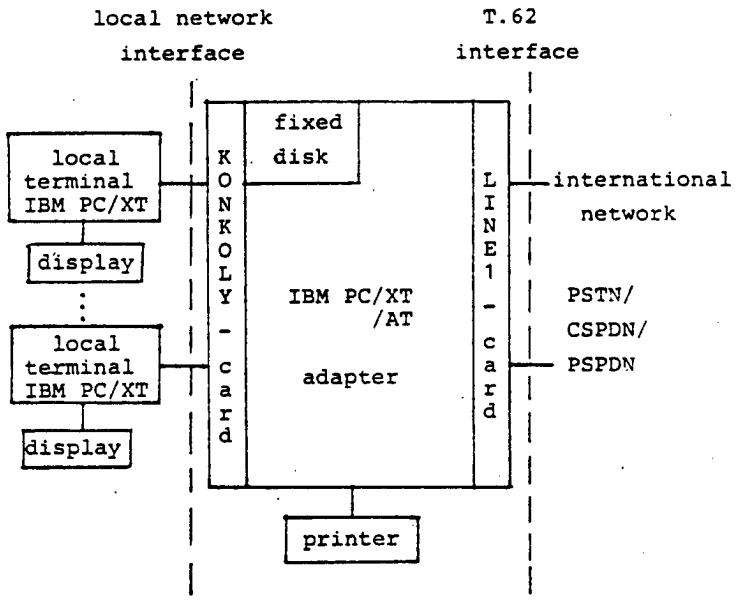


Figure 1. Hardware configuration

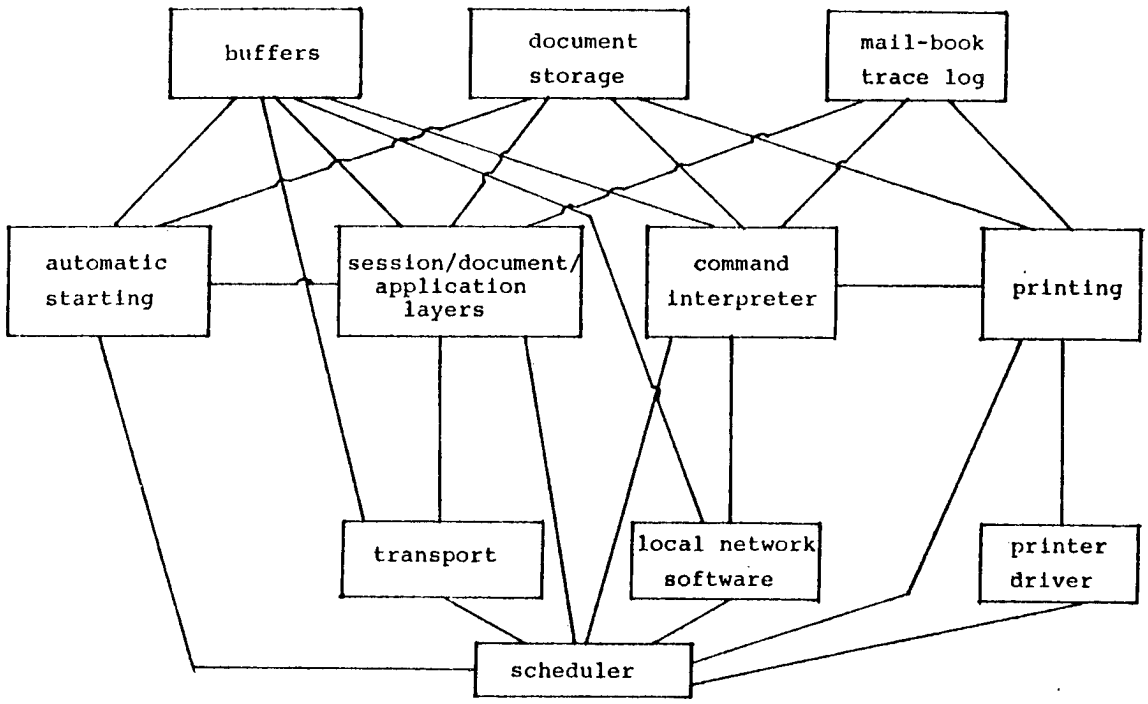


Figure 2. The structure of the adapter software

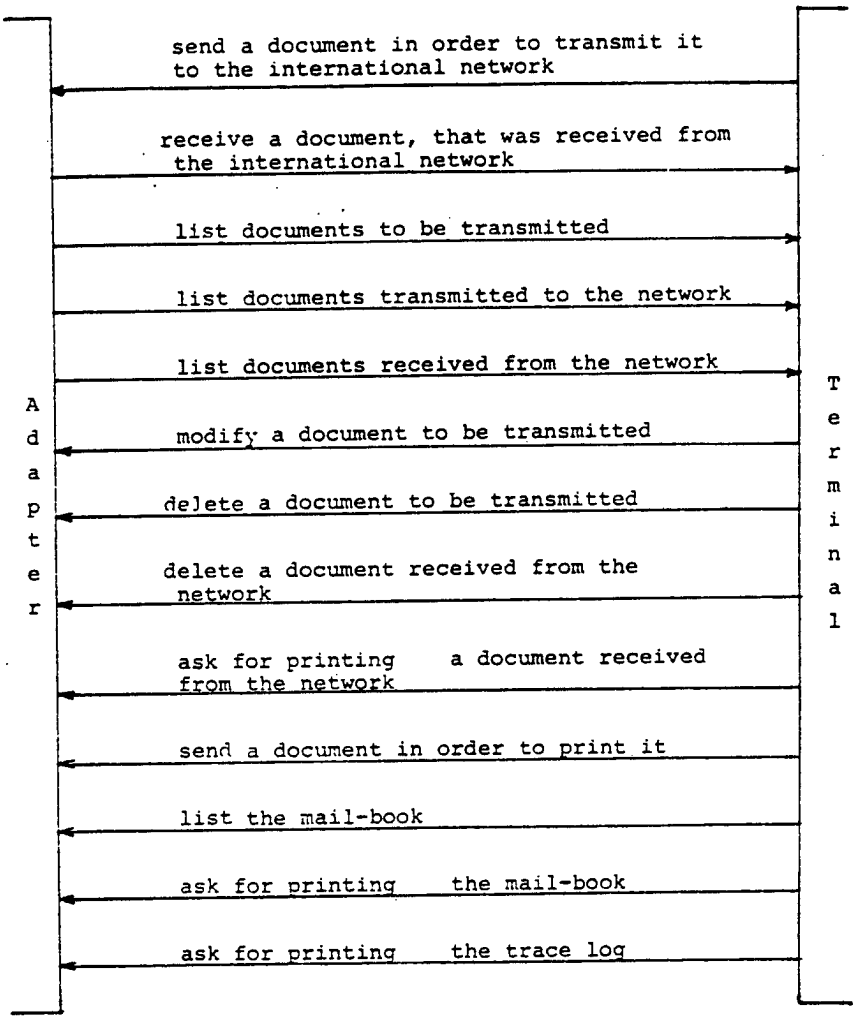


Figure 3. User commands

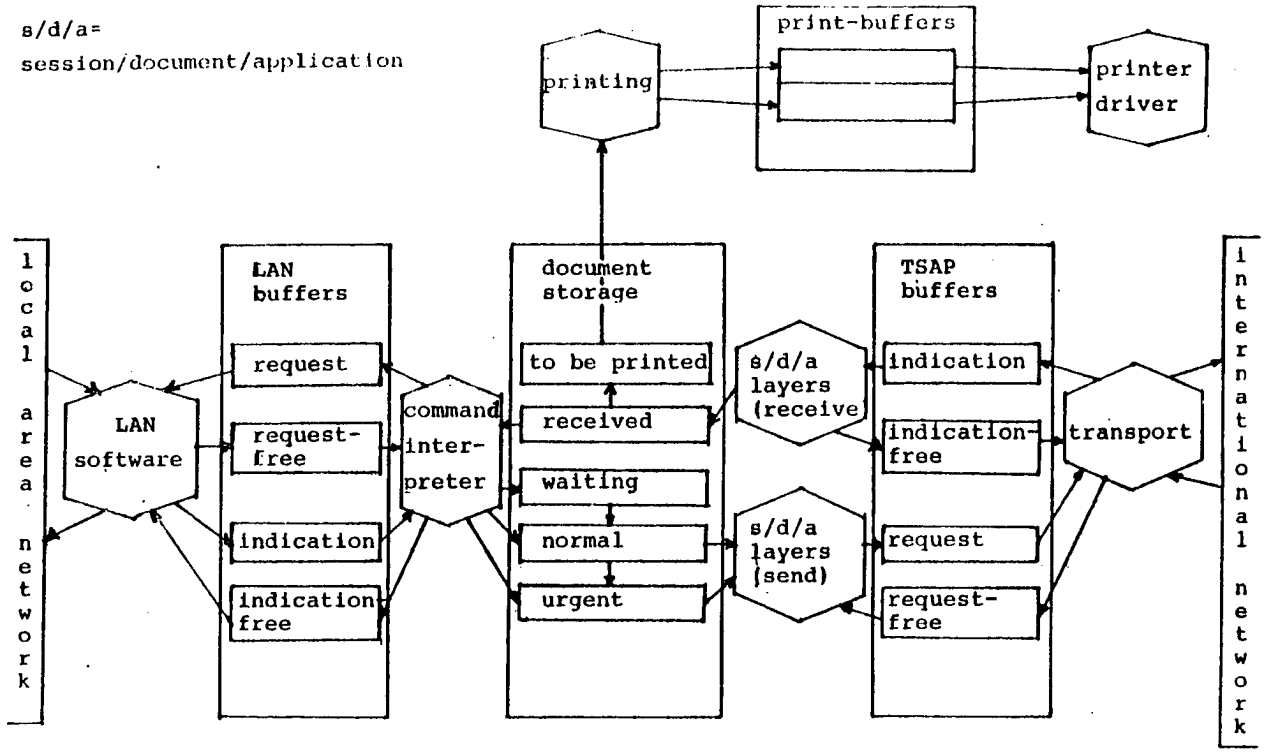


Figure 4. The operational scheme of the Teletex system

| data | producer | consumer |
|---|---|---|
| TSAP-buffers: | | |
| request-queue | document-sender, document-receiver | transport |
| indication | transport | document-sender, document-receiver |
| LAN-buffers: | | |
| request | command interpreter | LAN software |
| indication | LAN software | command interpreter |
| queue of documents to be printed | command interpreter | printing procedure |
| print-buffers | printing procedure | printer-driver |

Figure 5. The producer/consumer situations in the Teletex system

```
TYPE Element = RECORD
               finalState: CARDINAL;
               action    : PROC;     (*address of a procedure*)
               END;
VAR Table: ARRAY [state] [inputSignal] OF Element;

The evaluation of the state transition:

newState := Table [oldState] [actSignal] .finalState;
Table [oldState] [actSignal] .action;
```

Figure 6. The State Transition Table in Modula-2

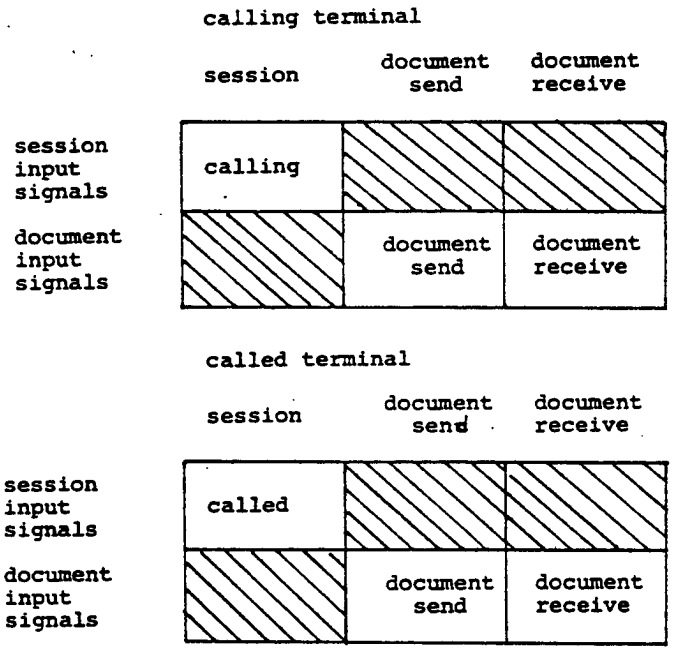


Figure 7. Modification of State Transition Tables

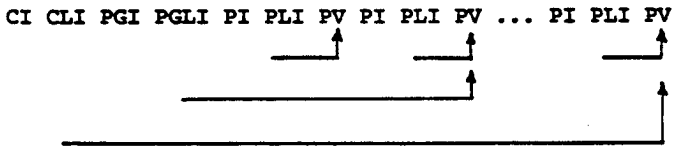


Figure 8. The parameter field

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# THE PC-188-S16 SERIAL I/O INTERFACE BOARD

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The PC-188-S16 is an IBM PC/XT and AT compatible 16-Channel I/O Interface Board which is controlled by an Intel iAPX-188 microprocessor. The board is coupled to the PC's host microprocessor via a dual port static RAM memory block. At the peripheral side the RS 232C interface is implemented. Debugging and future extensions are supported by Piggy Board extensions. The paper describes the hardware structure of the board and its software interface to the PC. An application of the board in industrial environment is also described.

## INTRODUCTION

In a geografically distributed system the key components of the technology are controlled by local microcomputers. In a hierarchically distributed control system these microcomputers are connected to a central microcomputer where the data base of the whole system is kept and processed and where the human interaction to the system is typically provided. For most applications the interconnections between the central microcomputer and the local microcomputers are implemented via serial links. Decomposing the task of the central microcomputer to interacting sub-tasks, one of them is the data concentrator function for the remote microcomputers. In a number of cases the telecommunication system exhibits star topology (Fig.1). For such a system the data concentrator function is implemented by a serial data multiplexer board (or some multiplexer boards) and a program running on the central microcomputer. In many applications an IBM PC/XT or AT personal computer is used as central microcomputer of the system. The PC-188-S16 is a 16-channel serial multiplexer board which fits in the I/O Channel Bus of the IBM PC/XT or AT.

## HARDWARE STRUCTURE OF THE BOARD

The main design goals were twofold. In one hand, to remove most of the workload associated with the physical handling of messages from the host microprocessor of the PC. On the other hand, to provide a great level of flexibility at the serial interface side. In addition, both XT and AT compatibility was also aimed.

To achieve the first goal, the board has got its own iAPX-188 microprocessor-based microcomputer. The interface to the PC host microprocessor is implemented by a dual port static RAM memory block. From the point of view of the host microprocessor, the board is represented by a 2KB read/write byte-accessible memory block and an interrupt request source.

The local iAPX-188 microprocessor works under the supervision of the host one. It cannot access directly to the PC I/O Channel Bus, rather it receives commands placed into the "mailbox" dual port memory by the host CPU and after having performed a command it responds by updating its status and asserting an interrupt request to the host.

To achieve the second goal, the i82530 Serial Communication Controller chip [1] was selected as intelligent communication device. The decision was motivated by the following features of the chip:

- two independent serial channels,
- Baud-Rate Generator and Digital Phase Locked Loop for each channel,
- diagnostic services (Local Loopback and Auto Echo) are provided,
- several data transfer modes (NRZ, NRZI, FM0 and FM1), two topologies (point-to-point and SDLC-loop), different data transfer protocols (asynchronous, byte-oriented synchronous and bit-oriented synchronous) are supported,
- it can be easily interfaced to the iAPX-188 microprocessor.

The XT/AT compatibility requirement was achieved by the byte-oriented interface to the dual port RAM memory over the I/O Channel Bus. The MEMCS16 and IOCS16 interface signals are not asserted. The base address and the control signals are jumper-selectable.

The hardware block diagram of the board is shown in Fig.2. The design takes advantage of the built-in functional units of the iAPX-188 microprocessor. The internal DMA Controller is shut down, because the data transfer rates of neither the dual port RAM interface nor the serial data channels do not demand its use. The implementation of the waiting times associated with the data transfer protocol is supported by the internal programmable timers. The enabling and timing of the on-board memory and I/O devices are based on the built-in Chip Select and Ready Logic. The internal programmable interrupt controller is initialized to master mode (non-iRMX mode).

The dual port RAM memory serves as a mailbox in the information exchange between the two microprocessors. The arbitration and multiplexer circuits are incorporated into the two VLSI Technology VT2131 chips [2], thus no additional circuits were needed to implement this function. If both microprocessor attempt to access to the same memory location, the arbitration logic resolves the contention by asserting the appropriate BUSY signal. The completion of the machine cycle of the lower priority CPU or of

the CPU which presents its request for a memory location being used by the other one is delayed by some forced wait states. Becouse of the limited number of forced wait states allowed in the PC, the PC side was given higher priority over the local CPU. For supporting the synchronization at software level, memory accesses to two dedicated locations assert interrupt requests at the corresponding sides. The 2KB dual port RAM represents a 4KB, jumper-selectable base address memory block mapped into the memory of the PC. It also represents 4KB for the local microprocessor and it is selected by the programmable MCS2 output signal of the iAPX-188. The interrupt request signal is connected to the IRQ3 line of the PC I/O Channel Bus (Serial Channel No. 2 interrupt).

The local memory consists of four 32KB chips. Either of them can be EPROM or RAM memory. These memory blocks are selected by the LCS, MCS0, MCS1 and UCS programmable output signals of the iAPX-188, respectively.

The eight i82530 SCC chips represent 32 I/O ports each. The I/O address decoder circuit is enabled by the PCS1 programmable output signal of the iAPX-188. The SCC chips are programmed for non-vector interrupt mode. The eight interrupt request lines are connected to the inputs of a i8259A PIC chip. The INT output signal of the PIC is connected to the INT0 interrupt input of the iAPX-188. The interrupt vector identifies the highest priority requesting SCC chip at a given instant of time. The three possible interrupt conditions per channel are searched and serviced in the common interrupt subroutine. A daisy-chained interrupt priority scheme could have been constructed by means of the SCC chips. However, this fixed priority scheme wouldn't be flexible enough for different applications. For example, equal priority for the remote microcomputers can be provided by programming the PIC in rotating priority mode.

The INT1 interrupt input of the iAPX-188 is driven by the interrupt request generated by the dual port RAM. The INT3 interrupt input is dedicated for program development and possible future extensions. Both the INT1 and the INT3 interrupt requests branch to the corresponding subroutines by means of internally generated vectors. The combined serial interrupt request has priority over the dual port RAM communication interrupt. The NMI non-maskable interrupt input of the iAPX-188 is not used.

For the sake of flexibility, eight serial channels are implemented on a Piggy-Board extension. This approach results in a lower cost solution if only eight channels or less were needed.

There is a provision for another Piggy-Board extension. The hardware and firmware support of the debugging services can be easily interfaced to the board in this way. In addition, further I/O and memory extensions to the board are also feasible.

At the peripheral side a limited version of the RS 232C interface (TxD, RxD, RTS, CTS, CD and signal ground) is implemented. The TI SN 75189A parts are selected for receivers and the TI SN 75188 chips for drivers, respectively. These driver and receiver circuits meet the requirements of the EIA RS 232C standard. The signal lines of the 16 channels are accessible at two 50-pin connectors on the PC chassis (Fig.3). In the cable assignment box the lines are distributed to 16 9-pin, RS 232C compatible connectors. The cable transmitter circuits are assembled in separate boxes for each

channel. Thus approppriate transmitter circuits can be selected for various applications for each channel and the modularity and flexibility of the product can be maintained at this level too.

## STRUCTURE OF THE SOFTWARE

The data concentrator can be characterised as an autonomous slave processor unit of the PC which unit in one hand, controls the data transfer and maintains the links with the remote terminals. On the other hand, it is linked to the user program running on the PC via a user interface program. In this approach, the user program works with a unified software interface and the details of the data transfer are handled by the program of the data concentrator.

Designing the program of the data concentrator the following aspects were considered:

- To remove the workload associated with the establishing and terminating of data links and information exchange with the remote terminals from the user program. However, data transfer can only be initiated by the user program.
- The program is to be of modular structure, easily changeable and reliable.
- The two lowest layers of the 7-layer ISO-OSI Reference Model are to be implemented.
- Special requirements of a real-time technological environment are to be considered.
- Provisions for debugging and self-diagnostics are to be provided.

The program consists of four main blocks (Fig.4). The main program decodes and carries out the commands issued by the user program. These commands are placed into the dual port RAM. In addition, following the power-on the main program runs the self-diagnostic program modules and initializes the programmable chips. At debugging, it invokes the program modules supporting the debug services.

The communication between the PC and the board is implemented via the dual port RAM. The memory map is broken up into dedicated fields which are as it follows: data field, command field, status field and debug field, interrupt flag and interrupt generating bytes. The sizes of the various fields are function of the different applications.

The tasks of the program implementing the data link layer are as it follows: establishing the data link between the nodes, terminating the data link between the nodes, generating formatted messages according to the selected data link protocol, sending, receiving and decoding of messages, timing, and recovery from error conditions.

A simple monitor program supports the development and debugging of the software system of the board. The monitor program decodes and executes the commands deposited in the debug field of the dual port RAM. By means of these commands the following functions can be performed:

- tq download a program from the PC via the dual port RAM,
- to set up breakpoints into the downloaded program,
- to start or to restart the downloaded program,

- modifying and displaying the local CPU registers,
- modifying and displaying the local memory registers.

In the course of the design of the programming language interface to the board two requirements were taken into consideration. First, let the program modules implementing the services of the board be invoked from the user program as procedures or functions. Second, a real-time application environment was also considered. The two main design principles came from these considerations are as it follows: each procedure immediately returns the control to the calling program which has to organize the waiting for the results of the called procedure. The second one is the use of the dual port RAM interrupt request to generate a software interrupt for the user program when the transmission or the reception of a data block has been completed in a serial channel.

The user interface consists of the following procedures: initialization, checking the status of a transmitted data block, transmission of a block, checking the status of a received block, and reception of a block.

SELF-DIAGNOSTIC FEATURES

These program services help the user to locate a bug in the multiplexer board.

- Exchange of a test data block with the PC.
  This operation is initiated by the PC. The data block sent by the PC CPU is copied to another dual port RAM area by the local CPU and then verified by the PC CPU.
- Test of the local RAM memory.
  A special pattern is written into the RAM and then checked by the local CPU.
- Test of the local EPROM memory.
  A checksum of 2B is re-generated and then compared to the contents of the checksum locations by the local CPU.
- Establishing a local loop.
  The i82530 can be programmed in Local Loopback Mode when the serial data outputs and inputs are connected to each other within the chip. Thus the programming and the internal state of the SCC, as well as a set of the local bus signals can be checked.

DEBUG SUPPORT

These program services help the user to locate a bug in the telecommunication system. All these tests are initiated by the PC. Manual interaction of the user is required. The status information is passed to the PC by the local CPU.

- Echo mode
  The data block sent by a remote microcomputer is echoed without any modification.

- External local loop

  The cable is disconnected and a short is placed between the cable transmitter and receiver terminals of the multiplexer board and then the data transmission and reception is checked.
- Cable checking (Remote loop)

  The cable is disconnected from the remote terminal and a short is placed between the corresponding data lines. Similar to the external local loop mode.

## APPLICATION IN HIGH STORE-HOUSE TECHNOLOGY

Two PC-188-S16 board-based data concentrators have been recently installed as part of a high store-house control system [3],[4]. The telecommunication system exhibits star topology. The remote microcomputers are Z80-based intelligent on-board terminals and LED display units. Eight channels of each data concentrator are used. The distance between the nodes does not exceed 200 meters. The data transfer rate is 9600 Baud. An asynchronous BSC protocol is implemented [4]. The minimal required capacity of the mailbox memory is 1KB, the memory map is shown in Fig.5.

According to the strong electro-magnetic noises in the application environment, current-loop drivers and receivers are choosen for cable transmitters. The cable transmitter circuits are isolated from the RS 232C interface chips by optocouplers.

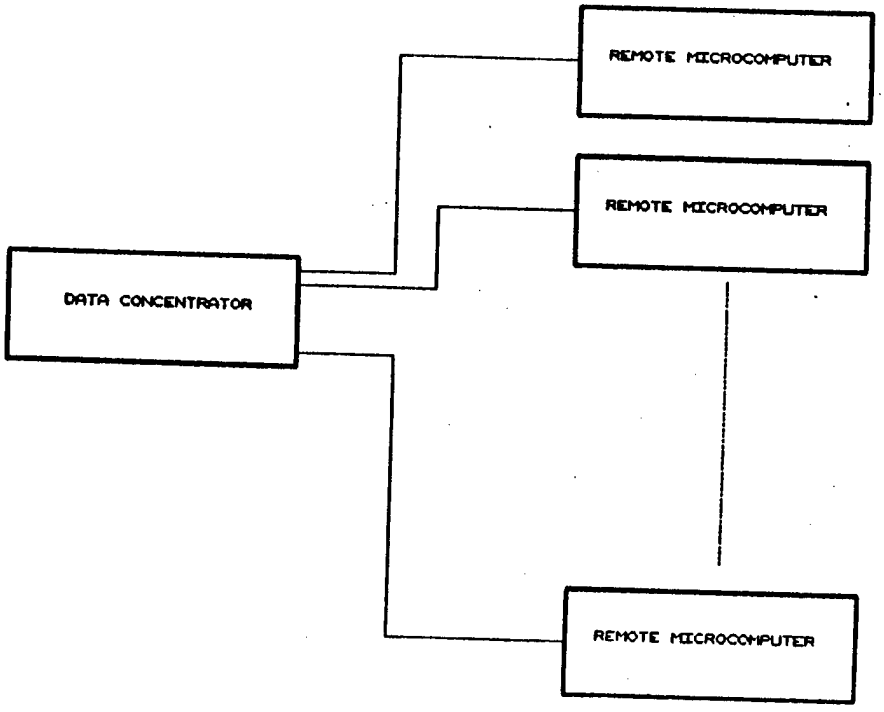


FIG.1

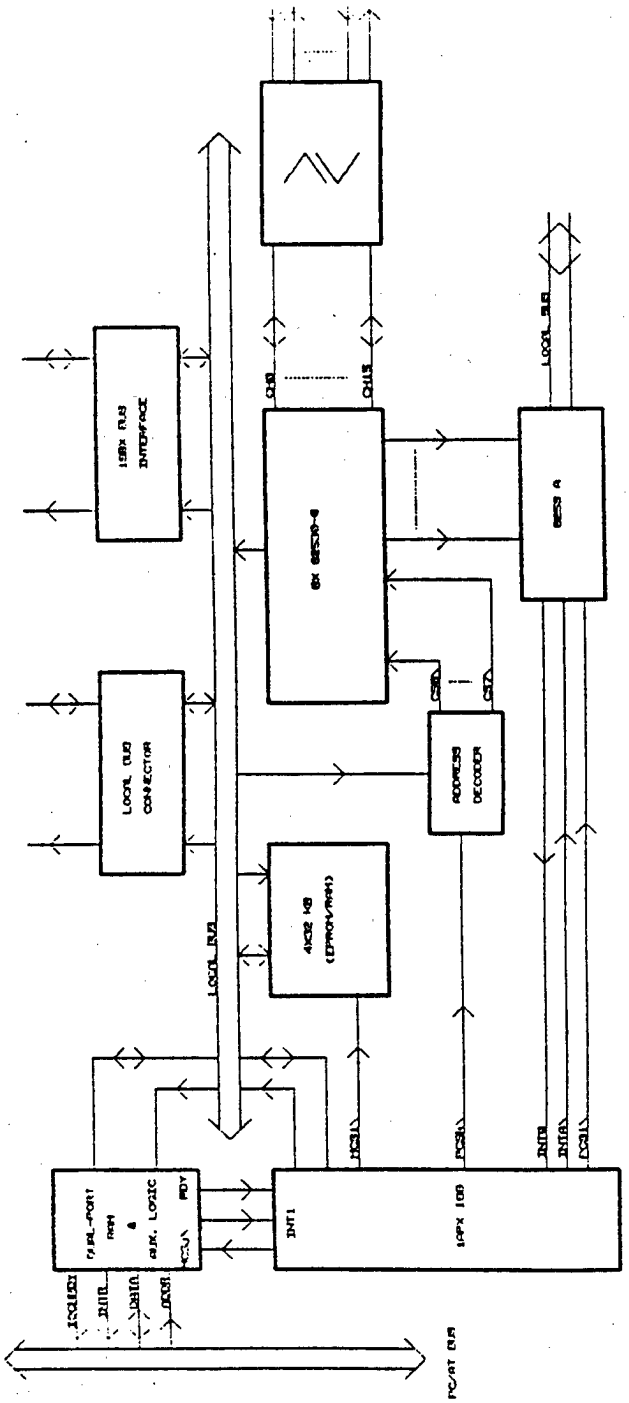

FIG. 2.

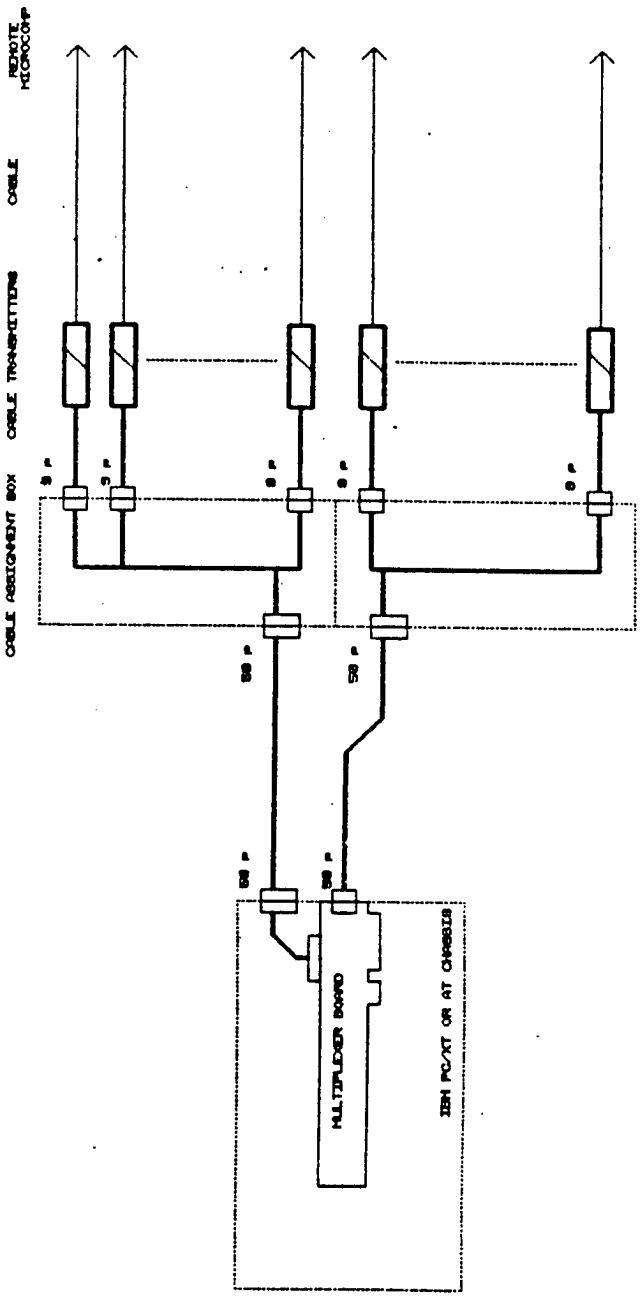
REMOTE MICROSCOPE
CABLE
CABLE TRANSMITTERS
CABLE ASSIGNMENT BOX
MULTIPLEXER BOARD
IBM PC/XT OR AT CHASSIS

FIG.3

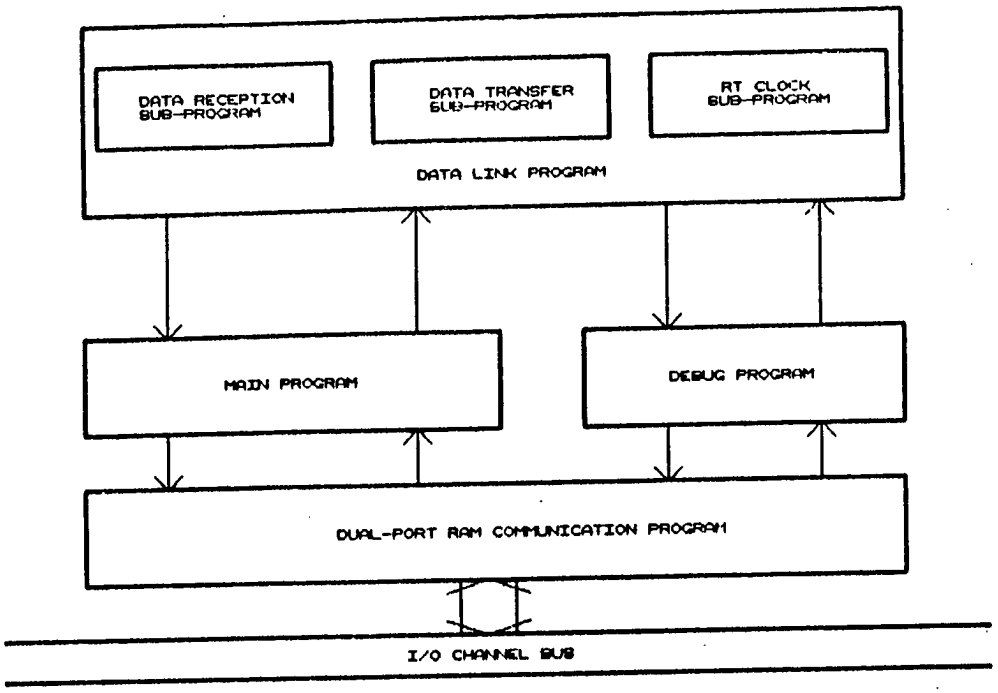
DATA RECEPTION SUB-PROGRAM
DATA TRANSFER SUB-PROGRAM
RT CLOCK SUB-PROGRAM
DATA LINK PROGRAM
MAIN PROGRAM
DEBUG PROGRAM
DUAL-PORT RAM COMMUNICATION PROGRAM
I/O CHANNEL BUS

FIG.4

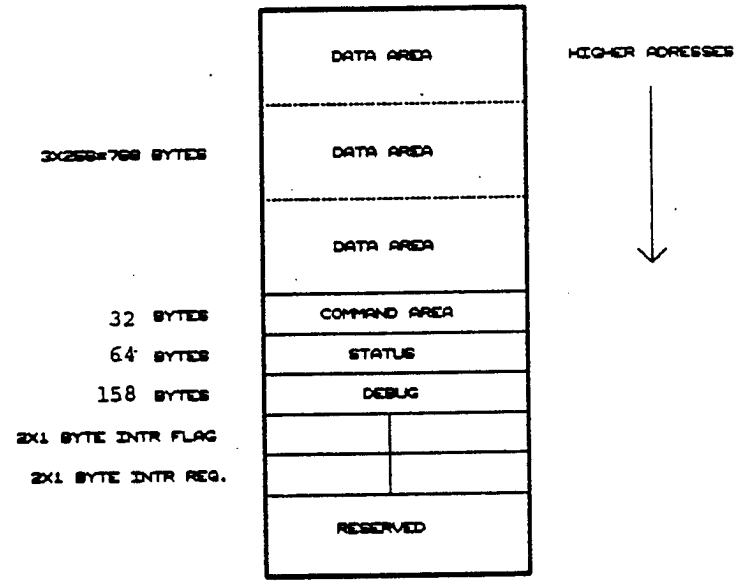
DATA AREA
DATA AREA
DATA AREA
3X256=768 BYTES
HIGHER ADRESSES
32 BYTES
COMMAND AREA
64 BYTES
STATUS
158 BYTES
DEBUG
2X1 BYTE INTR FLAG
2X1 BYTE INTR REQ.
RESERVED

FIG.5

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# VME-BUS AND FASTBUS SYSTEMS AND MODULES AT THE LABORATORY OF HIGH ENERGIES

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The hardware of modern elementary particle spectrometers and accelerator control systems are based on the 32-bit VME and FASTBUS standards.
The VME-bus (IEC.821 standard) allows one to introduce computer power equivalent to present-day supercomputer into the hardware of an experiment. The control system for a cycle generator of the superconducting synchrotron as well as a set of modules developed in the VME standard are considered.
FASTBUS is de facto an international standard for modern multichannel detector hardware. It provides the highest speed at a minimal registration channel cost. An analog information registration system of the SFERA spectrometer and a set of developed FASTBUS modules are described.

## INTRODUCTION

VME and FASTBUS 32-bit buses have found wide use in the hardware of modern elementary particle physics spectrometers and accelerator control systems.

A FASTBUS bus is used extensively in the hardware of multichannel particle detectors of superhigh energy physics spectrometers. It provides the highest speed to cost ratio for registration channels.

A VME bus (IEC.821) represents an international standard and allows one to introduce computer powers, which are

equivalent to present-day supercomputers, directly into experimental hardware.

FASTBUS[1] - and VME[2] - based systems and a set of modules have been developed at the Laboratory of High Energies.

## FASTBUS SYSTEM FOR ANALOG SIGNAL ACQUISITION

The architecture of a FASTBUS system makes it possible to build practically any superlarge system in a modular way.

At the Laboratory of High Energies a number of modern experimental installations are being constructed. They are designed for high energy physics research based on a wide use of the FASTBUS standard. Early developments in this standard in the SFERA[3] spectrometer are applied for studying multiple cumulative particle production in the geometry close to $4\pi$. Due to a low yield of the considered processes, the spectrometer has to process high intensity particle beams ($10^9 \div 10^{11}$ particles/s) what requires high-speed registration channels. The presence of thousands of information channels of a different type stimulates a search for new ways in the development of data acquisition electronics. The use of FASTBUS for solving the problems of fast data acquisition and selection has a lot of advantages over other existing standards. The system for recording analog signals of the SFERA spectrometer in the FASTBUS standard has been developed (see Fig. 1). Fast analog signals are transformed into a digital form by means of a FASTBUS 16-channel 8-bit ADC. The ADC conversion time is 40 ns. Information is read out from ADCs by a FIORI I/O register simultaneously from two channels. This module realizes a control protocol and transmits data to a bus for a FASTBUS segment. It also accomplishes a liaison with a computer. FIORI control commands and data are transferred through two 16-bit bidirectional I/O registers made as CAMAC modules. In the present scheme of liaison between FASTBUS and CAMAC buses the exchange process is controlled by an Elektronika-60 microcomputer. It is connected to the CAMAC crate containing I/O register modules by means of a branch driver and a crate controller of the A type. The minimum access time to the FASTBUS segment obtained in the system is 60 mcs. This is due to a rather low speed of the microcomputer and the FIORI module which requires a certain number of CAMAC cycles per one command. The total time of data processing is $1 \div 3$ ms which is in good agreement with time characteristics of similar systems.

The software of the system has a two-level structure which allows one to separate the tasks of information acquisition, current control, data processing and presentation. At a higher level of data recording and control the program works as a

task of the RT-11 operative system. It performs the following operations: module initialization, ADC coupling to the computer according to the FASTBUS protocol, data testing and preparation for subsequent handling which is realized by a background program. The set of MULTI-FB histogram programs has been used.

FASTBUS MODULES

A crate and FASTBUS modules have been and are being developed for the system under consideration and for the spectrometers prepared for UNK experiments. Among these are:
- a 16-channel 8-bit ADC with a 40 ns conversion time;
- a fast 8-channel ADC with a 8-bit 256-word memory;
- a 16-channel 350 Mc/s TDC;
- a 32x32-bit two-port buffer memory;
- a 32-bit parallel input shift register (8 words deep);
- a bus display module.

A number of auxiliary devices, including ventillation panel and crate mechanics, has been also developed.

VME-BUS - BASED CONTROL SYSTEM

A VME bus is widely used in advanced physics research as a base for designing data acquisition and data processing systems of elementary particle spectrometers, e.g., UA1 at CERN, as well as control systems of modern and future accelerators, for example, LEP/SPS.

In the last few years a microcomputer - based subsystem of accelerator cycle control has been in use in the control system of the superconducting synchrotron SPIN. The main tasks of the system are to control the bending magnets and lenses of the synchrotron ring and to synchronize accelerator elements and power supply current testing.

The system makes it possible to carry out studies at the synchrotron in two regimes: warm and helium-cooled.

Availability of just one computer in the system makes it impossible to correct the parameters of an accelerator cycle in real time. The generation of accelerator cycles was interrupted and a number of cycles was lost during an operative personnel dialogue and the subsequent calculation of power supply control code tables. The dead time of the system, $T_m$, was dependent on the time of operative personnel reaction and numerical values of introduced parameters. The use of a real-time system of the TR11-FB type did not solve the problem due to a low speed of the processor.

The goals of the system have been realized using a multiprocessor system liaisoned via a VME bus.

A new version of the accelerator cycle control system is shown in Fig. 2. Dialogue parameter setting-up and table calculations are performed by a Pravetz-16 PC. Both program sources of the system are coupled via a VME buffer memory module. The memory stores calculated results from the PC. These data are read out from the VME buffer memory within the space between accelerator cycles to the memory of the MERA-60 microcomputer. This makes it possible to start a new accelerator cycle with desirable parameters of power supply cycle pulses.

The system software consists of two subroutines written in FORTRAN providing a dialogue and table calculations. The program requires 64 Kbytes of RAM and runs under the control of DOS-16.

The dead time in the new system is smaller by a factor of 300. and any change of parameters just prolongs an interval between accelerator cycles up to an acceptable value.

## VME MODULES

For the system under consideration and others a set of VME modules has been and is being developed. Among these modules are:

- S.01 - a system controller with a synchrosignal generator, an arbitrator and a termination unit;
- P.01 - a four-channel serial register with an input organized according to the RS-232C protocol. It contains an Intel 8085 processor node with 32 k RAM and 16 k PROM;
- Z.01 - a 0.5 MB two-port DRAM accessible from a bus and a front panel;
- I.01 - a 16-bit parallel register;
- I.02 - a Q-bus system channel interface;
- I.03 - a V-bus adapter;
- I.04 - a DMA PC Pravetz-16 interface;
- I.06 - a CAMAC branch driver.

## VME-BUS IN DATA ANALYSIS AND PROCESSING

In traditional computers data are processed sequentially step by step. Physics and technological restrictions do not allow one in the near future to exceed significantly a value of 10 $\frac{\text{Mflops}}{\text{s}}$ and, consequently, limit the calculation speed.

A modular supercomputer based on multiple parallel 32-bit processors with a speed of 1 $\frac{\text{Mflops}}{\text{s}}$ is suggested. The processors are assembled to one supercomputer community by means of standard VME crates. The calculation process is supervised by a microVAX-11 host computer. Data I/O is implemented via

host computer peripheral devices. The software of the system is based on FORTRAN-77. The supercomputer can be integrated with the present JINR LAN through one of its ports to provide access to all users. The supercomputer allows one to calculate the most cumbersome tasks of elementary particle and accelerator physics, in particular Monte-Carlo and accelerator simulation.

The only limitation for solving the tasks is the possibility of their separation into parallel similar fragments.

Events in spectrometers are statistically independent. This situation allows one to handle them in a parallel way in a number of similar processors. In the supercomputer event data are distributed over numerous processors by a commutator. Each processor works with a similar handling program package. A relatively small volume of transferred data in comparison with the required calculation time allows one to involve hundreds of parallel processors in the handling process thus amplifying the power of the system almost in proportion to the number of used processors.

The architecture of the modular supercomputer consists of three main parts (see Fig. 3): a microVAX-11 host computer and its peripheral devices, a set of modular processors and LAN coupling means.

The host computer prepares calculation tasks for the modular processors, organizes the process of experimental data readout from magtape units or from the local network, distributes this information over the modular processors, accumulates and summarizes the results of data analysis obtained in the set of processors. The present architecture of the supercomputer is based on 72 modular processors distributed over four VME crates coupled to a control VME crate via star connection.

Each VME crate comprises up to 18 processors. The scheme shown above represents the first stage of the project.

The basic processor module of the supercomputer is composed of a 32-bit Motorola MC 68020 processor, a floating point coprocessor of the MC 68881 type, a RAM control chip of the MC 68851 type, a 8 Mb RAM, and a VME bus interface. Among the main software components are intercommunication programs, technological programs, e.g. a FORTRAN-77 compiler, and libraries of the applied programs (CERNLIB, HBOOK, ZBOOK, HPLOT, GEANT and so on). The software under development is a supercomputer communication routine.

The microVAX-11 system software is based on traditional means (VMS or UNIX) and routine software development tools.

The processor module system is a usual TMS monitor which provides a certain set of functions such as data interchange with the host computer, program errors and debugging.

## CONCLUSION

The use of 32-bit VME and FASTBUS buses allows one, in principle, to solve the tasks of data acquisition and most problems of data analysis in the field of elementary particle physics.

The development of VME - FASTBUS modules and systems seems to be attractive for use in applied and other fields of human activities.

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# IBM PC/XT Serial and Parallel Interfaces for experimental equipment connection

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The wide circulation of the IBM PC/XT personal computer, which has a relatively low cost combined with its unlimited number of software products make it very attractive for automation of physical experiments. At the same time the standard configuration includes only the serial RS-232C and parallel CENTRONICS byte interfaces only. This is not enough to effectively connect the necessary experimental equipment to the PC. To solve this problem two interface cards were developed at the Laboratory of Nuclear problems, JINR.

## SERIAL INTERFACE CARD

The electronics used in experimental nuclear physics is mainly in the CAMAC standard, this is why the PC interface was designed keeping in mind the existing equipment, which it must provide connection to.

Fast serial CAMAC-CAMAC link modules are wide-spread in our Institute, so the IBM PC/XT serial interface card with the same data transmission protocol and electrical parameters compatible with the existing CAMAC modules was developed.

This card consists of two identical channels each based on a 20-bit shift register. Parallel data are written to and read from the computer. Serial data are transmitted through the rear panel sockets. Serial input and output data transmission is provided via two coaxial connectors (one is for input and one for output) for link by means of coaxial cables, via the multipin connector for two twisted pairs (one pair is for input and one for output).

Data transmitting signals have the TTL levels in the coaxial cables. For the twisted pair connection the 75107 and 75110 driver and receiver are used.

The data transfer rate is 1.25 Mbits per second, i.e. it takes 16 microseconds to transmit/receive a 16-bit word. Clock pulses have the frequency of 10 MHz.

A transmitted word consists of 1 "Start" bit, 16 data bits, a "Flag" - bit and 2 "Stop" bits. The level of the "Start" bit corresponds to logical "1". The data bits are transmitted sequentially with the least significant bit first. The "Flag" bit can be used as parity bit, as "End of Message" sign, ets.

Each interface card channel is addressable by the computer processor as a two-byte word of the memory. One serial interface card occupies 16 bytes of the memory space. A base (segment) address may has a value of C000(hex) or greater and is chosen by jumpers on the card's printed board. The status byte, which can be read, defines the current status of the channels: receiver ready, transmitter ready, state of the "Flag" bits.

Word transmission to the line begins after the bus command of high byte writing. A channel is ready for reading when the "Receiver ready" bit of the status register is set. The special read command allow to initiate the transmission of the received data word back to the line.

The interface card can send the interrupt signal to the processor when one of receivers is ready. This feature is enabled by the jumper setting.

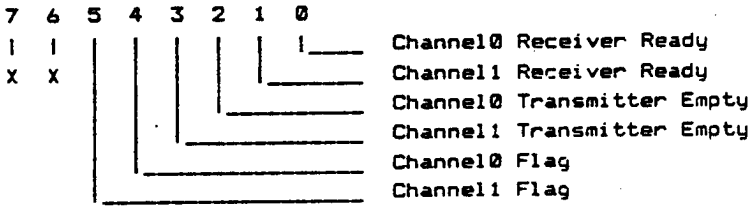
SERIAL INTERFACE TECHNICAL PARAMETERS

| | |
|---|---|
| Number of Channels | - 2 |
| Data transmitting/receiving format: | |
| Start | - 1 bit |
| Data | - 16 bits |
| Flag | - 1 bit |
| Stop | - 2 bits |
| Transmitting rate | - 1.25 Mbits/s ( 16 us/word ) |
| Distance: | |
| Twisted pairs | - 1 km |
| Coaxial cables | - 100 m |

Serial Interface Addresses Summary

| Address | READ Command | WRITE Command |
|---|---|---|
| Base:0 | Word from Ch0 | Word and Flag=0 to Ch0 |
| Base:2 | Word from Ch1 | Word and Flag=0 to Ch1 |
| Base:4 | Word from Ch0 and send it back | Word and Flag=1 to Ch0 |
| Base:6 | Word from Ch1 and send it back | Word and Flag=1 to Ch1 |
| Base:8 | Status Byte | |

Bits of the status byte:




PARALLEL INTERFACE CARD

This card includes the input and output 16-bit registers, which are read and written through the computer bus.

Data to the input register are entered via a 23-pin connector and strobed to the register by the external strobe signal. It sets the "Input register ready" flip-flop as well.

The input register accepts 16-bit data with the TTL levels, stores and transfers data to the PC bus in response to the read command. The transfer to the register is initiated by a strobe signal from an external source. The input register has also the "Gate" mode. In this case no strobe pulse is needed to transfer data to the register.

The computer read command forms a response signal to the connected equipment in the form of pulse and level. The "Input register ready" flip-flop is cleared at this moment. The external "End of Message" signal sets the appropriate flip-flop.

The output register is set by the write command from the PC bus and transfers 16-bit data to the 23-pin connector. The outputs are capable of sinking 40 mA to earth or withstanding + 30V with respect to earth. A request signal is sent to the connected equipment in response to the write command. It has the form of pulse and level. The "Output register ready" flip-flop is cleared at the same time. The external equipment must produce the response signal when it is ready to receive new data. This signal sets the "Output register ready" flip-flop.

A controlled multiplexer can form the interrupt signal to the PC bus. Outputs of the "Input register ready","Output

register ready" and "End of Message" flip-flops are the inputs for this multiplexer.

There is a 4-bit control register in the interface card. One bit defines the "Gate" or strobed mode of the input register, three other bits enable or disable passing the above signals to the interrupt line of the PC bus.

The status register allows the state of the control register and "Output register ready", "Input register ready", "End of Message" flip-flops to be read.

The interface card registers are addressed like the computer memory. The base address is adjusted by jumpers on the card.

# HIGHLY PARALLEL ARCHITECTURE FOR NEW GENERATION PPC

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Highly parallel architecture for personal supercomputers - PPC of a new class, is proposed. It is based on the recursive machines concept. The paper describes Recursive Personal Computer (RPC) multilevel virtual organization for VLSI implementation on microprocessors and ASIC. Prototype multimicroprocessor System 3M is presented.

The advance in design automation, integrated CAD in various fields, including VLSI and ULSI design require an ever increasing computer performance, tend to bring high computer power nearer to a designer's work place up to giving him such computers at his own constant and personal disposal. This is one of perspective application fields for personal supercomputers (PSC) - computing systems of a new class. For such PSC the high computer power in conjunction with the economical efficiency, the simplicity and the reliability in operation can be obtained only with VLSI high parallel computers. Recursive computer concept /RC/ is a prospective concept for high parallel computers design /1/ .

The recursive personal supercomputer /RPS/ internal organization can be described as a multilevel system of virtual machines /2/. Three basic levels can be distinguished: architecture level, logical structure level and hardware structure level / Table 1 /.

Architecture level is first of all, determined by the features of the RPS internal machine language, fig.1. The RPS internal machine language recursiveness is a language

recursiveness of this level language. A program in RPS internal machine language can be represented as a recursive structured object containing both operators and data.

Table 1

MULTILEVEL VIRTUAL ORGANIZATION OF RPS

| Characteristic features of a level | Levels | | |
|---|---|---|---|
| | Architecture level | Logical structure level | Hardware structure level |
| Recursiveness | Internal language recursiveness | System organization recursiveness | Topological recursiveness of structure |
| Program functioning environment in level machine language | Computational entity | Interacting modules system | Set of independently programmable modules |
| Memory | Shared | Distributed over modules | Distributed over modules |
| Processor and processes | Single process in /virtual/ processor | Set of processes in a module | Set of processes in a module |
| Resources limited | Unlimited resources | Finite resources | Quantitatively fixed resources |
| Switching functions in the system | No | Restructured logical channels between processes | Fixed hardware links between modules |

A program in internal machine language operates in a computing entity of unlimited resources. Each active program element is matched with its own machine component which is not shared by other active program elements /a virtual processor is matched with an operator, a data-object is matched with a cell of a mathematical memory unit/. The dynamics of a program operation and a delete of program objects during the computational process are directly revealed in the dynamics of a virtual machine structure. Virtual machine components directly interact with each other, there are no switching functions at the architecture level, fig.2.

The logical structure level comprises features of RPS system organization. A virtual machine of this level is represented by a finite set of modules which interact by

means of a switching system, fig.3. A module is a general-purpose component which is determined recursively within the logical structure. A module builtin facilities implement complete set of basic functions, such as data processing, computation control, data storage, in-system PSC is heterogeneous, so it can consist of various type modu - les. Each module implements a finite set of processes. At the logical structure level a switching system is an integral object, which implements a process-process inter-module interaction. This switching system operates in reply to explicit requests sent by the processes being executed in the modules.

The memory is distributed over the modules, where it is represented by a dynamically changing set of variable length linear segments. The processes operating in the module have a direct access to another module memory through interim-processes which are available in such module. Both an individual module resources and system resources as a whole are finite. The resources limitations are not quantative but they are qualitative by nature. They appear as a failure possibility for process resource request.

Hardware structure level represents a system as a set of hardware blocks interconnected by fixed links. The topology of this structure corresponds to some recursive determination. At the hardware structure level the RPS internal machine language is a set of module ma - chine languages. A program in each module operates separetly. The RC multiprocessor organisation is transparent from within a hardware module since existence or absence of any other modules is not represented in the module machine language semanties.

A recursive PSC module complexity /exept its RAM/ corresponds to a modern 32-bit microprocessor VLSI complexity. The RC heterogeneity enables to complement the modules by various types VLSI coprocessor. The paper gives a formal description of all the above-mentioned levels.

The RPC can be programmed using the expanded versions of conventional programming languages, which support a modular program organization and a separate module compilation.

The language extansions are represented by built-in functions /for system environment calls from program modu- les/ and by superlanguage Az which enables to specify a pro- gram as an asynchronous dynamic network of program modules processes.

The 3M multimicroprocessor system prototype of a recursive PSC, was built on bit-slice and single chip microprocessor LSI, fig. 4, /3/.

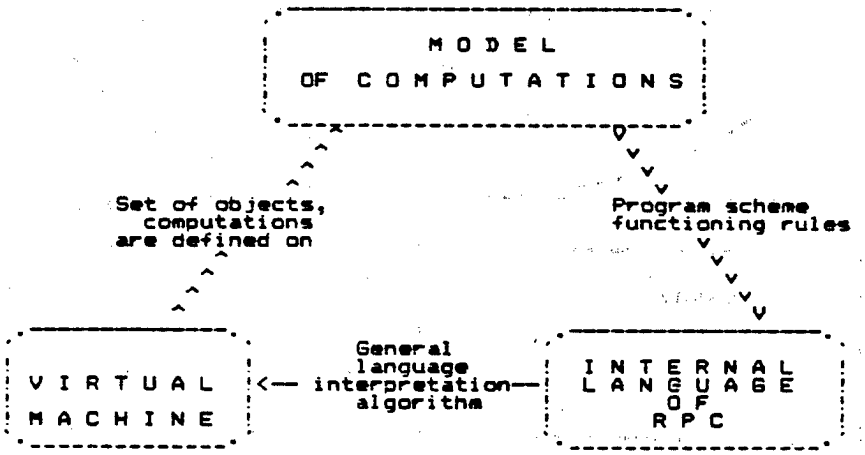
MODEL
OF COMPUTATIONS
Set of objects, computations are defined on
Program scheme functioning rules
VIRTUAL MACHINE
General language interpretation algorithm
INTERNAL LANGUAGE OF RPC

Fig. 1.

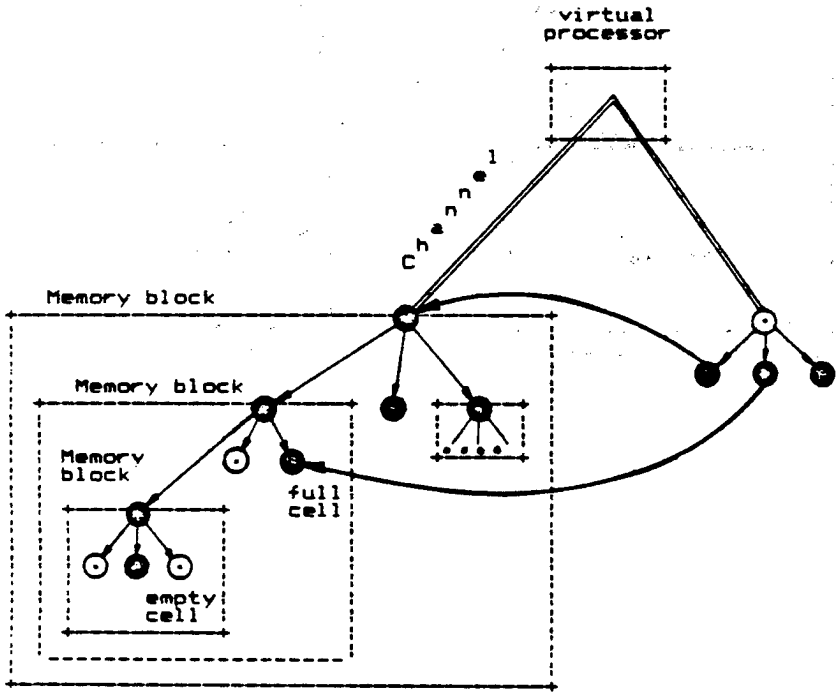
virtual processor
Channel
Memory block
Memory block
Memory block
full cell
empty cell

Fig. 2

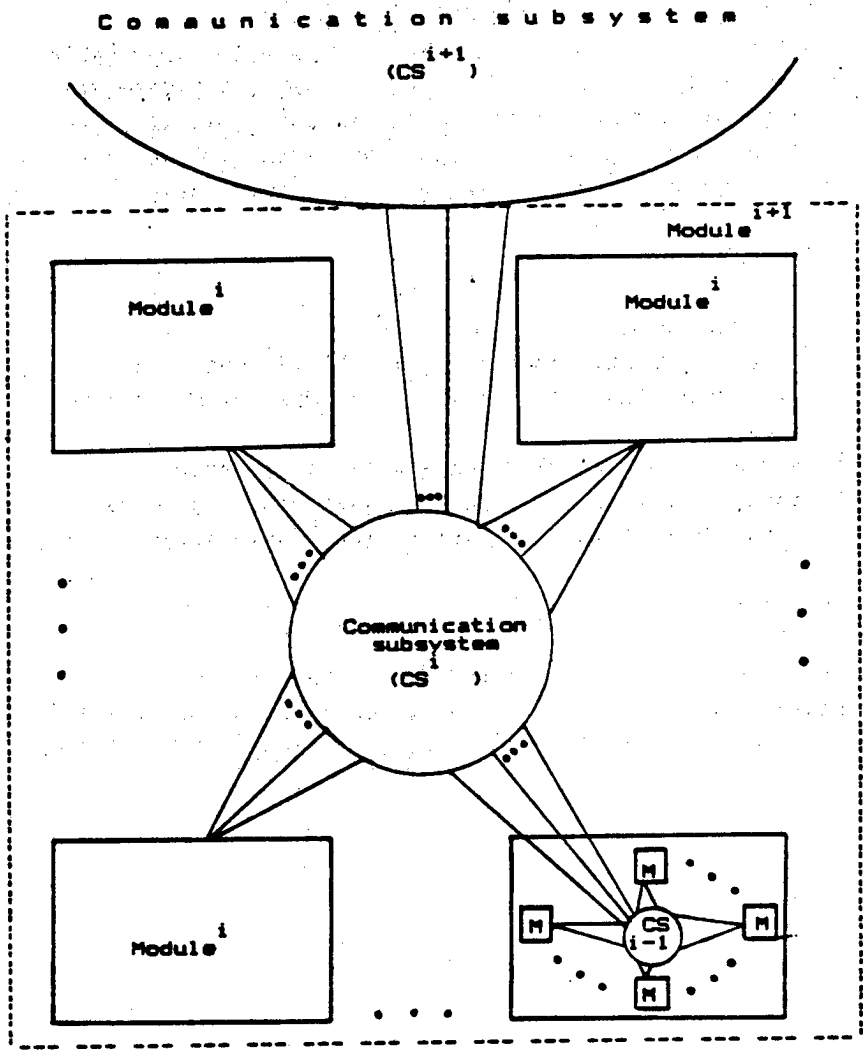
Communication subsystem
(CS i+1)
Module i+1
Module i
Module i
Communication subsystem
(CS i)
Module i
M
M
M
M
CS i-1

Fig. 3

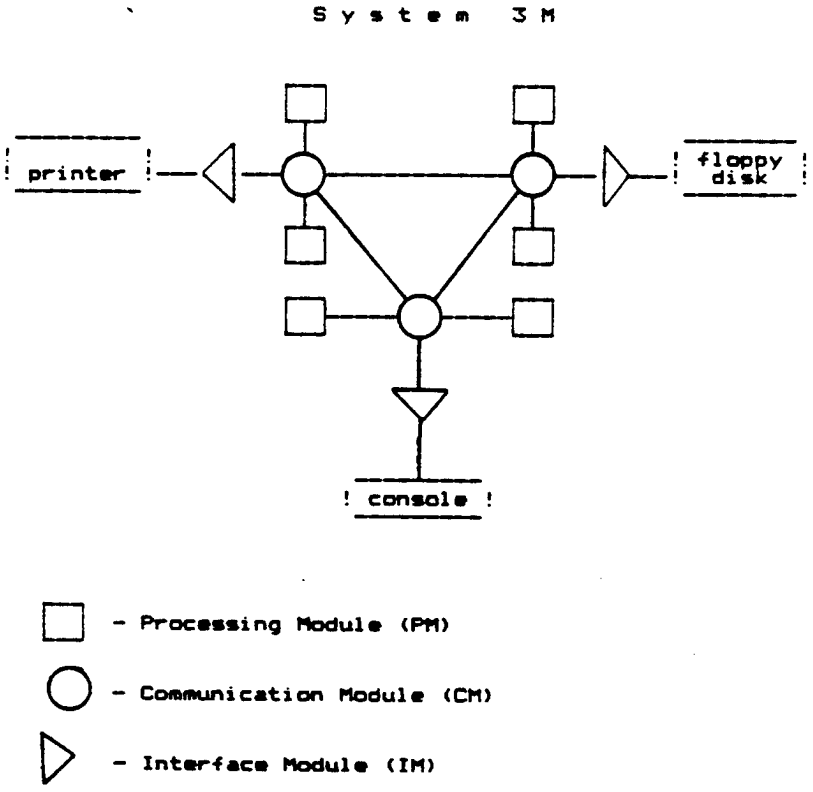


Fig. 4

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# Dual microprocessor-based load-sharing microcomputers

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Great increase of requirements to the communications systems involved the necessity for considerable complication of the software used and thus the necessity to increase control computer capability. There are known systems using multiprocessor control unit technique.E.g. X system of Plessey(UK). The multiprocessor system architecture is based on the multiplexer concept with the loading shared processors controlled by the operating system.

Mass production of LSI microprocessor sets with large functional capacities,their low cost,flexibility and accuracy of digital data processing methods made these microcomputers (MC) system elements,providing the base for production automation,communication and measuring systems,etc...

For the last 20 years computer aids found an especially large application in communication engineering.With the stored program control,various computer-based communication systems enable the users to have still increasing number of services and fully automated process to use both the equipment itself and subscriber lines and terminals.Communication systems use both one-chip microcomputer Intel 8080,8038,8045,8086(Soviet series 580,1810,1816),MOTOROLA 6800 and multi-chip(sectioned) microcomputer-aided microprocessors,e.g.Series AMd 2900(Soviet 1804).

Great increase of requirements to the communications systems involved the necessity for considerable complication of the software used and thus the necessity to increase control computer capability.

There are known systems using multiprocessor control unit technique.E.g. X system of Plessey (UK).

The multiprocessor system architecture is based on the multiplexer concept with the loading shared processors controlled by the operating system.

Alongside with the task to increase the capability of control units in communication systems it is necessary to solve the task to improve their reliability(standard requirements - less than 2 hours delay for 40-year operation).

There are also systems using different methods of processor duplication with the purpose of increasing control units reliability:

1. "Hot reserve" - when 2 computers handle the same problems and compare results.On error detection the faulty computer is disconnected.This method is used in ESS exchanges (USA )and KWANT exchanges(USSR).

2. Dynamic function separation - when tasks are handled under the common monitor control.The 1st computer begins the handling and the 2nd ends it.On monitor request the response is given by the free computer.It is used in private exchanges,such as developed by THOMSON.

3. "Static function separation" - when each computer is responsible for executing its own functions.During the task handling process there is a continuous data exchange.

4. "Loading-sharing" - when 2 computers share the tasks as they are delivered on the principle of randomness.During the operation the computers keep exchanging status data.If one computer breaks down all the loading may be handled by the other.

Our enterprise in cooperation with ALCATEL(France) developed and realised for manufacturing dual microprocessor-based load-sharing modular microcomputers series 2901 and 2904.

Basic specifications.

- digit capacity - 32/32 - bit data bus,16-bit address bus;
- microcommand execution time is 244ns (execution time for commands depends on the number of microcommands,realising the given command and memory access time;
- realization of 48 Assembler USE-11 commands;
- 1 level and 32 sublevels of interruption;
- load-sharing operation: if one computer fails all the tasks are handled by the other with automatic error localization;

- reliability: downtime probability is less than $0,5 \cdot 10^{5}$ for the period of 140 years;

- amount of equipment : 10 $PCB_s$ 234 x 365 x 27 mm and 2 power supplies.

The $PCB_s$ assignment.

- ALU - 2
- Microprogram control unit - 2
- Intercomputer communication unit - 2
- Programm memory - 4
- Supply voltage - + 5 V

power used - up to 100 W

- Periphery:
  - teletype,
  - display,
  - optionally,cartridge tape drive.

General application: it is used as the EAX subscriber concentrator control unit.Also it may be used as control unit for other radio electronic systems requiring large capability and reliable functioning control units.The architecture of each microcomputer is standard as recommended by AMD.

The intercomputer communication unit(LIC) is of greatest interest.It consists of the microcomputer start-stop system and provides data exchange between 2 microcomputers and between each microcomputer and non-duplicated periphery.The data exchange involves execution of the following functions, realised by the proper equipment modules and software.

- " Intermicrocomputer communication" : two-direction 64-bit register,holding data on two microcomputer exchange.
- " Computer status word" - 16-bit register,holding data on two microcomputer status(working,disabled,testing,etc.). One bit change in the 1st microcomputer status word generates the 2nd microcomputer interruption signal.
- "Exclusion" - enables to settle data source access conflict between two microcomputers.
- "Interruption pulse generator" - interruption of 2 microcomputers every 4 ms with the shift of 2 ms.
- "Two microcomputer control" - enables alternate switching of 2 microcomputers in case of simultaneous accidental stop.
- "Time delay latch" - checks the control over microcomputer and periphery exchange.
- "Timing-pulse generator" - excludes the influence of one microcomputer on the other.

Task handling is associated with the necessity for intercomputer message exchange.All these messages have the format of 4 16-bit words.The last word is the check word.Data

exchange process goes in the following sequence:
for example,microcomputer A initiates interchange and simultaneously writes datd into its LIC for transmission;and on completion of writing it creates interruption LIC 1 in microcomputer B.

Microcomputer B carries out reading and then creates interruption LIC 0 in microcomputer A,cancelling interruption LIC 1.

Introduction of this microcomputer communication unit made it possible to increase the control unit capability by 50% and ensure high reliability of system operation.

Microcomputer testing with a few dozen of $EAI_s$(more than 2 thousand microcomputers produced)proved them reliable and the chosen technical decisions correct.

# HIGH SPEED CLUSTER LAN FOR PROFESSIONAL PERSONAL COMPUTERS

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Technical characteristics and economical limitations for high speed LAN based on PPC in network CAD and CAE systems demand new, not multidrop line, arhitectures. Cluster LAN arhitecture LENCLUSTER is proposed. High speed LANs for PPCs with total throughput from one up to tens of Mbyte/s may be constructed. Hardware for LENCLUSTER LAN construction - Network Communication Controller and Communication Network Adapters for PPC, are described.

## 1. Network Development Systems with PPC

Professional Personal Computers (PPC) are widely used for computer aided design and engineering. Microprocessor-based systems design is an example, [1]. Most systems are product of the collective design. Stand alone workstations does not correspond to collective nature of a design process. It is necessary to turn to based on LAN Network Development Systems (NDS). LAN must provide efficient designers interaction, shared resources usage (expencive i/o devices, magnetic tape and disc storage, computer and information resources). High speed devices, large storage, on-line information exchange capacity, response time limitations for user-system interaction call for high speed network. Rigid economical limitations are caused by PPC characteristics: network cost (per node) must not exceed 10-15% of PPC cost.

Homogeneous office LANs, based on a sole multidrop line of some kind, suppose uniform information exchange streams throughout the network. Such LANs are not efficient for

NDS with PPCs: they are either too expensive (e.g. Ethernet), or too slow. High speed LAN design for NDS must take into account specific character of design process organization, of information streams, of typical NDS nodes location.

## 2. Cluster LAN Architecture

The main principal of cluster LAN "Lencluster" design - multilevel heterogeneous system of interacting subnets, fig.1.

The low hierarchy level clusters are primary subnets, connecting small groups of user nodes with high-rate in-group communication (4-8 nodes typically). Designers team is usually devided into such groups. Members of a group are usually placed in the same room, at the distance not exceeding 10-15 meters from each other and from the group shared devices. Communication within a group is most intensive. It demands 5-10 Mbit/s (0,5-1 Mbyte/s) transmission speed within level 0 cluster.

Next level cluster are used for communication between groups of one team, working at the design. Communication between clusters are used for casual access to shared information resources. The inter-group communication rate is much less then in-group communication. Transmission speed requirements for level 1 clusters - 0,5-1 Mbit/s. Distance between user nodes (i.e. for members of one team) can be limited by 100-300m.

Next level cluster connection corresponds to a different nature of user nodes interaction. It corresponds to interaction between teams - not hourly communication in there current work, but time to time requests-answers, issue requiment, etc. Transmission rate about some tens of kilobits per second is quite acceptable here. At this level, distance between nodes is large - they are spread all over facility.

## 3. PPC Cluster LAN Components

Component set for high speed cluster LAN was designed. They include Network Communication Controller (NCC), Communication Network Adapter (CNA) for user node PPC and Network Software Package.

NCC designed for in-cluster communication between PPC and for inter-cluster communication for low-level clusters. NCC maintain direct communication with up to 8 nodes by parallel channel at the rate of 1 Mbyte/s. NCC implement packet

switch communication with packet intermediate buffering in NCC (1000 packets by 256 bytes per second), channel switching or adaptive switching.

NCC is based on transputer module RT841, built on high rate bit-slice microprocessor, [2]. RT841 include 4 Kbyte RAM, 4 Kwords program PROM, 8 i/o units. RT841 with apropriate software in PROM implements NCC - a communication system for 8-node cluster. For distance less then 15 meters, parallel multicore cable (typicaly - flat cable) is used. For distance up to 300m the serial link - optical fibre cable, is used (~ 8 Mbit/s). In this case the different plug-in i/o units are used in NCC.

CNA attach PPC to LAN Lencluster. One-board CNA implements data link protocol.

The third level cluster is a low-rate one. Special phisical links throughout a facility for these level cluster is not justified. PABX can be used as communication entity in this case, [3].

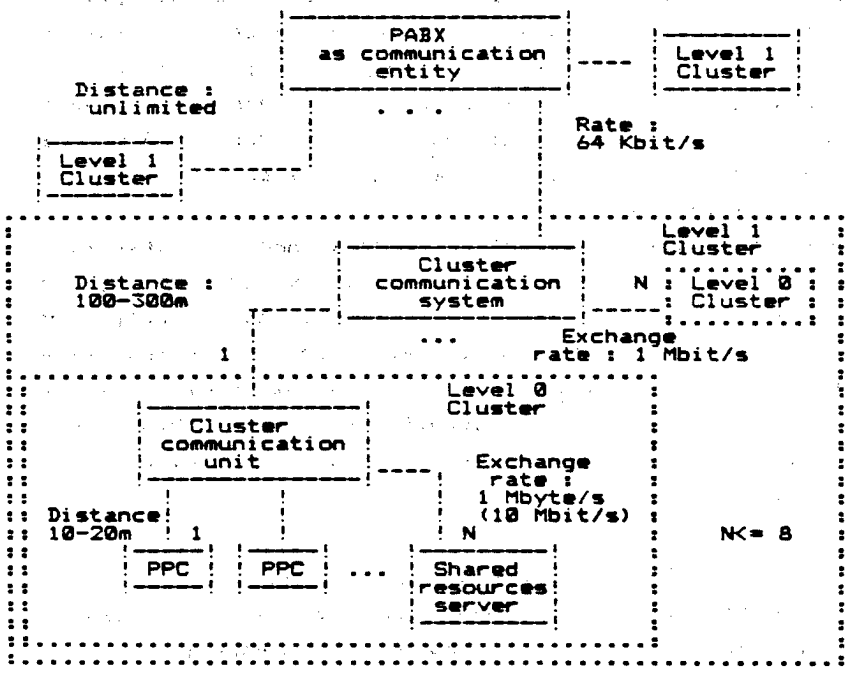


Fig. 1. "Lencluster" LAN

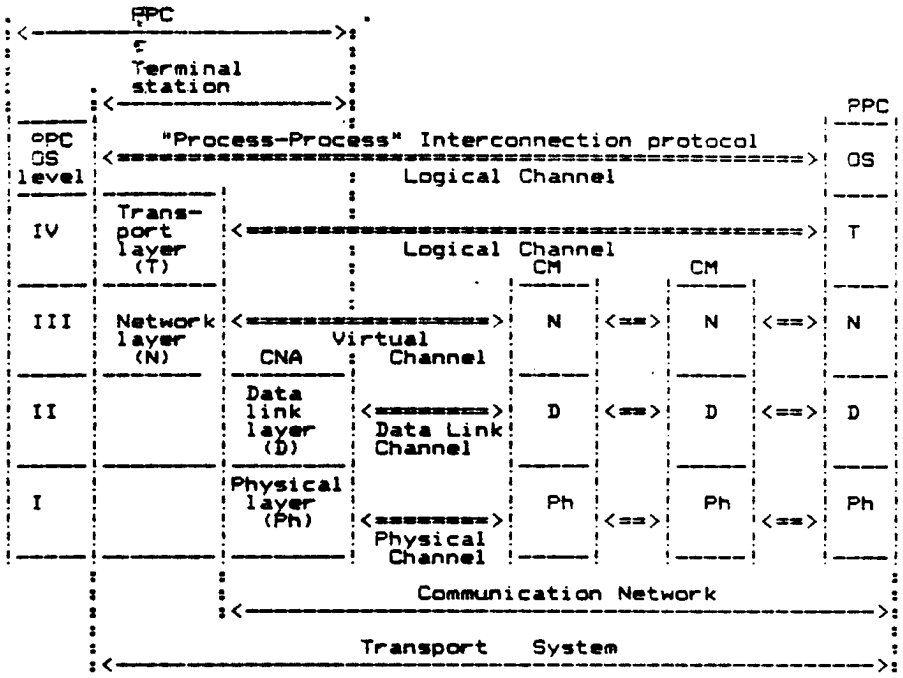


Fig. 2. Protocol Architecture of "Lencluster" LAN

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# PC-BASED REAL-TIME IMAGE PROCESSING SYSTEM

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## ABSTRACT

Prior to nowadays the evaluation of visual information was not feasible in many applications due to the inadequate performance of available systems in spatial resolution, number of grayscale levels, processing speed or storing capicity. Until now image acquisition and processing at an acceptable rate for real-time applications have not been possible or investigations resulted in a too expensive experimental system.

The paper describes an image processing system, which is based on the following key elements:

- Research work on digital picture processing algorithms generally applicable and realizable by hardware.
- The advent of new VLSI technology made it possible to implement a PC-based modular image processing system with a hardwired vision processor implementing many of the operations at video-rate.
- Special sensors, mechanics and lightning systems has been developed providing extremely high resolution.
- The easy modification of application level software makes it possible to solve different kind of picture processing problems.

The article describes an expert system capable to digitize, evaluate and store industrial radiographic pictures of high optical density and signal-to-noise ratio, and an industrial quality control system [2], [3].

## INTRODUCTION

In the past few years, real-time image processing using high resolution digital pictures has become a rapidly growing field in factory environment which involve decision making based on interpretation of digital images. Tasks of this kind include defect recognition or quality control of materials. Programmable flexible automation (robotics) is also a field of growing importance for real-time image processing [1]. The term "real-time"

can be defined as the processing of data is at the same rate as visual information obtained by means of the camera.

Machine vision systems are already on the market [6], [8]. Most of them operate only on binary images. The reason is the huge amount of data that every gray-scale picture contains. For example an image of 512x512 8 bit pixels gives over 2 million bits of information. A method to get more computing power for a system is to use multiple processors. Many special purpose architectures have been proposed over the last years. There are several papers and books published on the subject [5], [7]. The advent of VLSI technology has made it possible to implement complex computational elements large memories at a reasonable cost.

Implementing some of these general ideas:

- efficient preprocessing algorithms were found, most of them can be realized at video rate
- we designed a special-purpose modular hardware
- the prototype PC-based vision system was succesfully used in nondestructive testing industry and textile automation

## THE DIGITIZATION OF NDT RADIOGRAPHS OF WELDING *

The radiograph of a welded joint is a negative film. Human evaluation of radiographs is made as follows: the film is put above an illuminating lamp and analysis is made rather subjectively. Typical shape of defects, their size and occurence frequency are analysed and the results are compared with a series of data given in tables.

Importance of exact judgement is not measurable in money in such cases as testing of welded joints used in nuclear power stations or in pipeline systems.

Further disadvantage of the present film storing and evaluating systems:

- the quality of the films deteriorates gradually, basic information partly disappears, for this reason to determine the increase of defects in case of periodical tests is practically impossible. Without this information the evaluation of remaining durability is very difficult.

Prior to nowadays digital image enhancement of NDT radiograph was not feasible because of the high spatial resolution, optical density and signal-to-noise ratio of NDT films.

A Radiographic Expert System RADEXSYS was developed aiming to solve these problems. The main components of the system can be see on Fig.1. The performance capabilities of RADEXSYS are illustrated by the following key features:

. Film width: 0...300 mm
. Resolution: 1024...4096 pixel/line (depending on the type of CCD line scan camera)
. Bit depth : 8 bit/pixel
. Scan time : 20 sec for a 1Kx8K sampling matrix

* This work is supported by A4GM, Hungary.

. Display options: 256 grayscale video
256/256K pseudocolor video
1024x768 pixels
. Backup : VHS interface with 30 to 100 film/casette storing capacity

Digital film imaging reduces image analysis time, improves the accuracy of area and density measurement. An analitical "defect map" is generated containing type and 2D/3D informations belonging to these defects. Interactive evaluation is supported by contrast manipulations and hardware zoom, roll, pan. The system also faciliates easy storage, retrieval and transmission of images.

The data-base of RADEXSYS helps to standardize the decisions of NDT radiographers.

The final result is an overall increase in productivity for radiographic inspection.

VISION FOR TEXTILE AUTOMATION *

The inspection of materials constitutes an important factor in textile industry too. These inspections, are very labour intensive. As human inspection can become unreliable and rather expensive, we developed the system "TEXYS" which can automatically inspect some quality features of textiles. The system is capable of detecting all defects of material which can be separated by a "window" scanning on the binarized picture. A greater region of actual video data with 8 bit/pixel resolution can be stored in a temporary video buffer - for more sophisticated off-line software evaluation of interesting details. A high resolution monitor can visualize the grayscale and binary video data or the results of feature finding test for the specific region of interest. In case of relatively low speed of materials, this graphic illustration can be done on-line with the inspection routines for the whole picture.

The system consists of three principal components (Fig.2).
. IBM AT compatible based real-time image processor
. High resolution CCD line camera
. Testing mechanism

Microcomputer
All system procedures are carried out via the microcomputer which is composed of the following units:

Image acquisition unit
- interface for one Fairchild CAM 1600R CCD line camera (or equivalent)
- analogue contrast enhance
- exposure time: 0.7-70 msec/line approx.
- pixel rate: max. 5 MHz

* This work is supported by Flexys, Hungary

- maximal speed of material [in m/s]: cca. 1.5 x camera resolution [in mm]
- 8 bit A/D conversion
- digital shading correction
- 10 bit D/A output (for illumination control)
- operation is syncronised to the speed of material

Real-time feature finding unit

- two programmable 8 bit comparator for adaptive thresholding
- texture analysis in a local window
- feature detection with up to 8 parallel algorithms
- standard or user definable algorithms
- x,y of defects stored
- histogram evaluation, maximum grayscale value and the coordinate in the line are stored
- temporary buffer for 8 bit/pixel video, binary video and selected features

IBM AT compatible computer

- minimum hardware requirements:
  1 Mbyte RAM, Colour Graphics Adaptor, Colour Monitor, Printer, Hard Disk, 1.2 Mbyte Floppy Disk Drive, and at least two available slots
- optional hardware:
  Enhanced Graphics Adaptor (ATI VGA WONDER)
  High Resolution Monitor (NEC Multisync XL)

Line Scan Camera [9]

- Fairchild 3456-element line scan camera Model CCD 1600R
- Bayonet-mount lenses with local lengths of 25 and 50 mm.
  Interfacing for other kind of cameras is also possible.

Testing Pad

- mechanism for material movement
- adjustable speed in the range of 0-1 m/s
- speed transducer with TTL pulse output
- adjustable homogeneous illumination (special fluorescent light source)

SOFTWARE

- menu driven
- written in Microsoft C, Microsoft ASM, running on IBM AT compatible micro-computers (DOS 3.00+)
- modular software with three levels:
  I. hardware handling level
  II. feature finding level
  III. user level

MAIN FUNCTIONS OF "TEXYS"

Calibration of optical system:

- with the help of visualization of line scan camera information the user can bring into focus the whole optical system
- automatical setting of exposure time and illumination due to material transparency and material conditions
- correction of the inhomogenity for the whole optical system

System parameter set up:

- automatical system configuration takes into consideration of the following parameters: camera resolution; set of features to be detected; etc.
- standard and/or user defined algorithms can be implemented

Display options:

- grayscale video
- binary video
- user-definable pseudocolour
- features detected on the image
- calibration curves
- alphanumerical information
- resolution with optional monitor: 1024x768 pixels

Examples for real-time image processing [see Fig.4]:

- shading correction
- adaptive thresholding
- filtering
- sharpening
- edge detection (Laplace, Sobel, Huckel, etc.)
- erosion
- dilation
- mask matching
- user-definable convolution
- evaluation of global geometric properties
- etc.

Algorithms can be chained and/or paralelly executed.

System outputs:

- "stop mechanism" message
- "defect detected" message
- type of defects
- coordinates of defects
- storage function
- display function
- standard and/or user defined algorithms can be implemented.

## VIDEO-RATE PREPROCESSING

Several image processing algorithms were found useful both in RADEXSYS and TEXYS, therefore their video-rate hardware implementation has been made. Some of these algorithms are indicated on Fig. 3. The Fig. 4. gives examples for basic convolution masks and global geometrical properties [4].
This real-time feature finding unit can work up to 8 Mpixel/sec rate. Parallel and/or serial connection of basic algorithms results in more complex features and greater, more "global" window size.

## CONCLUSION

This paper has considered an IBM AT based image processing system which has a very high data throughput rate (up to 5 Mbyte/sec) for the chosen, generally applicable preprocessing algorithms. The implementation of the hardwired vision processor has been outlined. The paper described two applications implemented in the field of industrial inspection, but the need for the fast processing of large amounts of pixel data became evident in biomedicine, robotics, CAD and OCR techniques too.

## ACKNOWLEDGMENT

I would like to express my sincere gratitude to Prof. P. Arató, Head of the Dept. of Process Control and to all my colleauges in this field for their invaluable help.

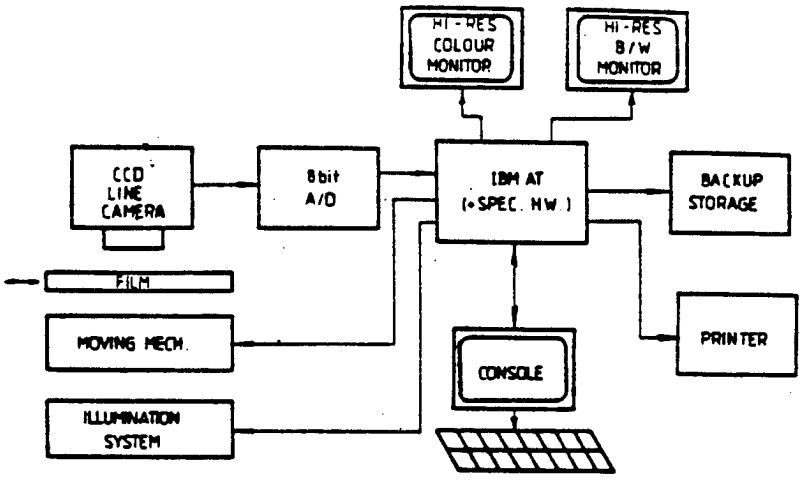


FIG.1.

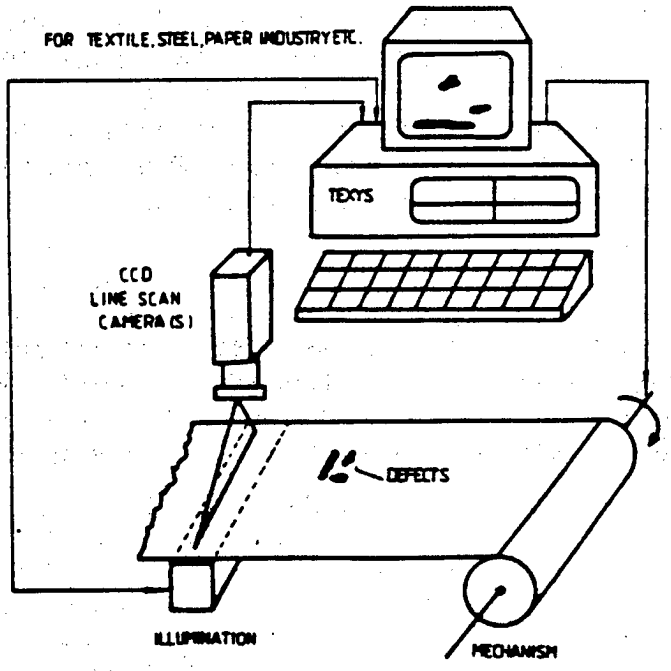
FOR TEXTILE, STEEL, PAPER INDUSTRY ETC.
TEXYS
CCD
LINE SCAN
CAMERA (S)
DEFECTS
ILLUMINATION
MECHANISM

FIG. 2.

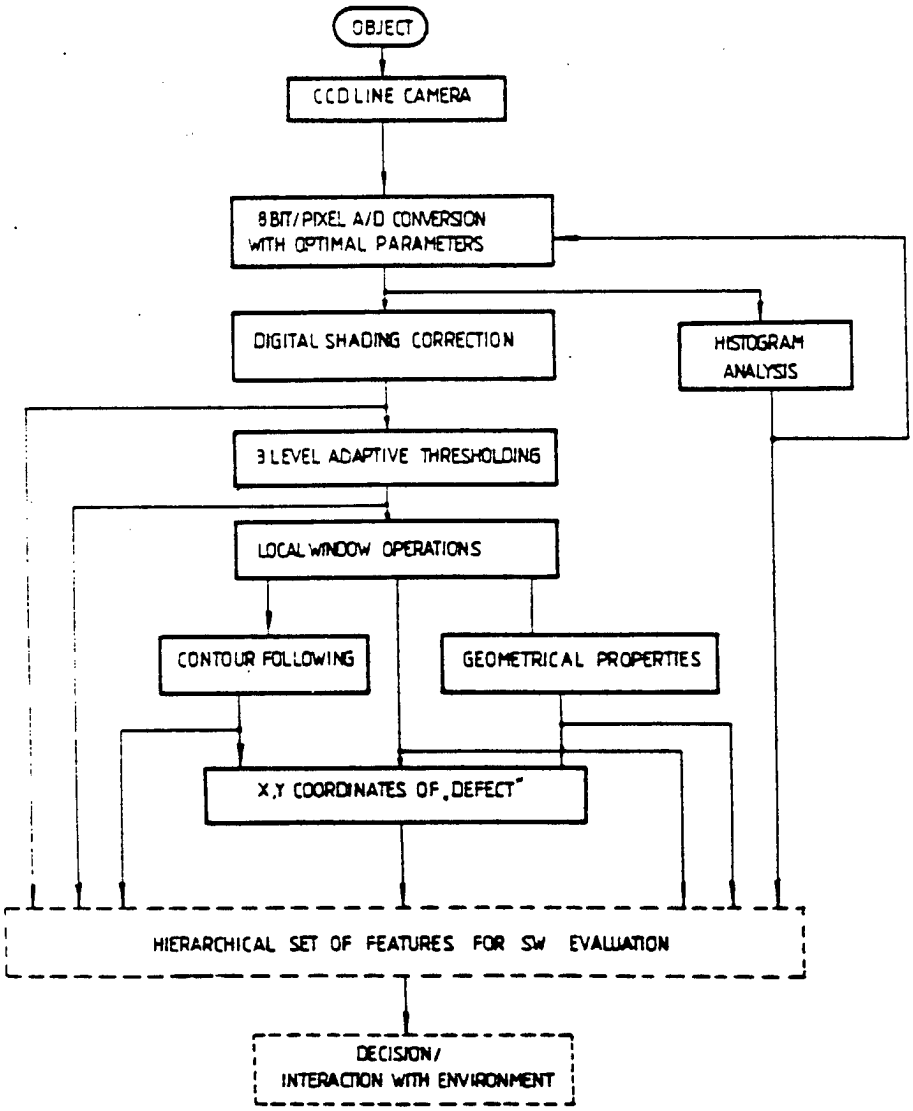
OBJECT
CCD LINE CAMERA
8 BIT/PIXEL A/D CONVERSION WITH OPTIMAL PARAMETERS
DIGITAL SHADING CORRECTION
HISTOGRAM ANALYSIS
3 LEVEL ADAPTIVE THRESHOLDING
LOCAL WINDOW OPERATIONS
CONTOUR FOLLOWING
GEOMETRICAL PROPERTIES
X,Y COORDINATES OF „DEFECT"
HIERARCHICAL SET OF FEATURES FOR SW EVALUATION
DECISION/ INTERACTION WITH ENVIRONMENT

FIG. 3.

## CONVOLUTION MASKS (EXAMPLES):

| | | | |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 |

AVERAGING

| | | | |
|---|---|---|---|
| -1 | -1 | -1 | -1 |
| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |

HORIZONTAL EDGE DETECTION

| | | | |
|---|---|---|---|
| -1 | 0 | 1 | 0 |
| -1 | 0 | 1 | 0 |
| -1 | 0 | 1 | 0 |
| -1 | 0 | 1 | 0 |

VERTICAL EDGE DETECTION

| | | | |
|---|---|---|---|
| -1 | -1 | -1 | 0 |
| -1 | -8 | -1 | 0 |
| -1 | -1 | -1 | 0 |
| 0 | 0 | 0 | 0 |

LAPLACE GRADIENT

| | | | |
|---|---|---|---|
| 1 | 1 | 1 | 0 |
| 1 | (1) | 1 | 0 |
| 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 |

EROSION
PIXEL=0 IF $\Sigma < 9$

| | | | |
|---|---|---|---|
| 1 | 1 | 1 | 0 |
| 1 | (0) | 1 | 0 |
| 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 |

DILATATION
PIXEL=1 IF $\Sigma > 0$

## GEOMETRIAL PROPERTIES (EXAMPLES):

| | |
|---|---|
| $Z_{i,j}$ | $Z_{i,j+1}$ |
| $Z_{i+1,j}$ | $Z_{i+1,j+1}$ |

CRITERION FUNCTION:

$$V_{i,j} = Z_{i,j} + 2 \times Z_{i,j+1} + 4 \times Z_{i+1,j} + 8 \times Z_{i+1,j+1}$$

STRUCTURE VECTOR:

$$V^T = [V_0, V_1, \ldots V_{15}]$$

$$\text{AREA} = \sum_{k=0}^{7} V_{2k+1}$$

HORIZONTAL PROJECTED PERIMETER $= V_2 + V_4 + V_{10} + V_{12}$

8-NEIGHBOUR EULER NUMBER $= V_8 - V_5 - V_{12}$

ORIENTATION $= V_6 - V_9$

ETC.

FIG. 4.

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# COMPUTER AIDED FACILITY
# for INFRARED SENSOR TESTING

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Current technical capabilities in the field of infrared sensor testing makes it possible to use such instruments in space research. Testing these sensors is a necessary precondition for their use. In light of the number and variablility of the sensors to be tested, it is necessary to develop automated procedures to measure the two main parameters -responsivity and detectivity- of these devices. At present sensor testing facilities make use of Personal Computers. It was completed with further OEMs. In some cases special slots had to be developed for example, the ADC, the DMAC, and the programmable power supply, clock generator, and clock amplifier. The efficiency of the PC and its accessories is determined mainly by the quality of the software. The structur of the software allows additions made by the user, for instance certain subroutines.

## INTRODUCTION

We describe here a computer aided facility for infrared sensor testing, called IRMA. The purpose of this paper is to describe this test facility, its structure and its operating software. IRMA was developed in the Institute of Space Research of the G.D.R.

Fourier-spectrometers and multispectral cameras are commonly used in our institute. Our scientific staff is interested in using IR-channels in various purposes, for example, earth observation and deepspace researches.

The first step before using IR-detectors on board of a spacecraft is to prepare the sensor for the special application, and to determine its main characteristics. This step is quite complex and can be very expensive. Because of this, as well as the various kinds of IR sensors used and the diversity of the research projects, the key issues regarding hardware design were modularity, flexibility and programmability.

IRMA is used to determine the following characteristics of an IR-sensor:

- R responsivity ¨ V/W }
- $\lambda_{peak}$ spectral peak response ¨ $\mu$m }
- $\lambda_{cut-off}$ spectral cut-off ¨ $\mu$m }
- NEP noise equivalent power spectrum ¨ $V^2/Hz$ }
- SNR signal-to-rms-noise ratio ... SNR
- $D^*_\lambda$ normalized detectivity as a function of frequency ¨ cm $\sqrt{Hz}$ / W }
- variation in responsivity within a detector area

PRINCIPLES of MEASUREMENT - THE NARROW BAND METHOD

The conventional method to measure responsivity and detectivty is an electrical selective one. The radiation is modulated by a chopper, passes the monochromator and is detected by the IR-Detector. Using Lock-in-voltage techniques, the detector gives the mean value of the incoming radiation. Stray radiation does not influence the measurements because the DC parts of the radiation are surpressed. By using Narrow-band-methods a high signal-to-noise ratio is reached.

This is an effective method for measuring the response of one-element detectors. However currently technologies are concentrated on manufacturing focal plane arrays with many detector elements. These are arranged together with different readout techniques. Such detector assemblies cannot be assessed effectively by this method.

THE BROAD BAND METHOD AND MEASURING PROCESS

The responses of assemblies with more than one detector and various readouts (hereafter called sensors) can be measured by broad-band methods. Instead of modulation the incoming radiation passes a shutter. The reference level is obtained with the shutter closed.

The responsivity is determined in two steps. First the irradiance E is measured with the help of a detector whose responsivity is known.

Then the output of the detector being tested is measured with a source of known irradiance. From this the responsivity can be calculated.

The measurement of irradiance "shutter opened" minus "shutter closed" gives the reference irradiance:

$$\Delta E(\lambda) = A_{DET}^{-1} \left[ (P_{SO}(\lambda) + P_{SO,D}) - (P_{SC}(\lambda) + P_{SC,D}) \right]$$

During these two measurements stray radiation $P_{SO,D}$ and $P_{SC,D}$ coming from the tube must be stable. The same procedure must be used to obtain the output of the sensor. With this measured output, the responsivity can be calculated as follows:

$$R_{DET} = \frac{\Delta I_{DET}}{\Delta E_{ref} * A_{DET}}$$

Certainly the requirement for stability of the stray radiation must be maintained. The temperature of the shutter and the disturbing radiation of the tube can be treated as a linear correction.

The detectivity is proportional of the reciprocal noise-equivalent power (NEP)

$$D^*(f) = \frac{\sqrt{A_{DET} * \Delta f}}{NEP}$$

The NEP is defined as that radiation power whose signal-to-noise ratio in the sensor output is one. If we measure the noise current by its power spectrum $S_N(f)$ the normalized detectivity can be calculated as function of electrical frequency:

$$D^*(f) = R_{DET} \sqrt{\frac{A}{S(f)}}$$

The advantage of this way determining $D^*$ is that we get the detectivity not only for a few frequency points but for the whole spectrum. To reduce the dispersion of the spectra many measurements are made to smooth the detectivity function.

## THE AUTOMATED TEST FACILITY

The demands which the planned test facility must meet can be summed up as follows: we must design an automated test facility which performs measurements of the responsivity and the detectivity by the broad band measuring method independent of the read out principle of the sensor.

Current techniques in the field of automatic sensor test facilities involve computer assistance. The measuring and control

devices are connected with a Personal Computer (PC) to provide a complete and powerful measuring system. The PC must perform different tasks as follows:

-control the power and clock supply of the sensor, the performance of the radiation source, the wavelength of the radiation, the positioning of the sensor and the temperature on special measuring points.
-measure the output signal of the sensor and of the calibrating sensor.
-process the data both mathematically and statistically.
-store the results on Floppy Discs for long term archiving and further study.
-show the results not only in columns of numbers but in an easy to survey manner on a graphic display or by a plotter.

## COMPONENTS of MEASUREMENT FACILITY

Fig.1 shows the arrangement of the optical and electrical components in the system as constructed. It has to accomplish the measurements on the basis of strong modularity and under conditions which allow effective measurements to be made. The configuration consists of the following units:

. black body or other radiation source
. shutter
. monochromator
. slit output focusing optics
. xy-movable platform
. reference detector
. sensor to measure
. cooling system
. analogue electronics
. measurement computer

Each of the main components is controlled by a single board computer (SBC) which is connected with the measurement computer by serial interfaces. These subprocessors control the real time process requirements of the various physical components, and the measurement computer will be free from the real time conditions of the periphal units.

The measurement computer is busy mainly with data acquisition, data processing and controling the timing of the measurement.

## THE OPTICAL AND PHYSICAL ARRANGEMENT

We now present a brief descriptive summary of the components actually used in this system.The black body is a round, grooved

graphite block about 100 square centimeters in area. Its temperature can be adjusted with a precisition of ±0.2K within a range of 300K to 500K. The control unit is the SBC and is based on a special estimation algorithm.

The shutter is arranged between the radiation source and the monochromator. This shutter also acts as a black body and so its temperature is measured. The positioning of the components is executed by a SBC-aided optical physical arrangement (OPA) controller.

After passing the shutter, the radiation enters the grating monochromator and its output is focused by mirror optics on the focal plane.

The alternative positioning of the reference detector (sensor) is realised by a movable xy-platform. This platform is adjusted by the OPA-controller in two directions. The positioning commands give the measurement computer the timing requirements of the measurement process.

## THE ANALOGUE DATA CHANNEL

The analogue data channel is the interface between the tested sensor on one the hand and the digital data channel - the PC - on the other. It is connected by a parallel interface and controlled by an SBC which gets its instructions from the PC. In the switch-on-moment the SBC performs an initialisation of the analogue data channel to prevent indeterminate states.

The modularity principle is especially important in the design of the analogue data channel because almost every new sensor type demands special conditions for the clock and power supply. Therefore programmable slots for filters, power supply, clock generation and amplification had to be developed.

The power supply slot allows the adjustment of four voltage sources with 20 Volts deviation in 256 or 4096 steps by the PC. If more voltage sources are needed one can use further power supply slots. In this case further addresses have to be arranged in the computer programme.

The programmable clock generator is the central station for all clocks used by the sensor, the analogue data channel and external. It contains a programmable basic clock of maximal 2.5 MHz and a memory for eight different clocks with a capacity of 1,024 states per clock. The SBC loads the memory in the switch-on-moment. The computer programme of the PC also loads the memory and moreover the user can influence every state of every clock. It is of course possible to use more than one programmable clock generator.

The programmable clock amplifier adapts the output level of the clock generator (TTL) to the demanded input level of the sensor. There are the same adjustment possibilities as in the power supply slot.

The analogue data channel also has the task of converting the analogue sensor output signal into a digital signal for the PC. This is done by the analogue digital converter slot. It works on the basis of the AD 574 which reach a converting frequency of 40 kHz and a resolution of 12 bits.

## THE COMPUTER

Given the strategy of building the system in a modular manner, it was decided that insofar as possible off-the-shelf, commercially available, subsystems would be used. The modular configuration computer A 5120, made by ROBOTRON, GDR, supports such a strategy.

The structure of the computer-unit is shown in figure 2. The standard functions of the computer-system, such as interaction, display, storage and restorage of data, printing and plotting are satisfied by the A 5120.

The first step in testing is to obtain data from the detectors and store it in a suitable form for subsequent processing. This function is realized with a direct memory access (DMA).

The DMA-controller card is like all other house-made cards in the PC-format of the A 5120-computer. The DMA-controller connects the computer-part with the analogue data channel and makes it possible to reach data transfer rates up to 830 kBytes per second. The system clock frequency of the computer is 2.5 MHz.

The A 5120-computer provides all instructions for the peripheral SBCs of the analogue data channel (ADK), the optical-physical arrangement (OPA), and the programmable black body (SK). The SBC is connected with the A 5120-computer by serial interface.

The floppy disc is used for restoring the data for subsequent analysis in the IRMA-system or off-line processing in another computer. The results of the test are recorded in the form of tabular listings and printer plots.

The measurements and the sensor-characteristics can be represented as functions of time, frequency, wavelength or locality.

A comercial graphical subsystem with a colour monitor expands the possibilities of the IRMA-system. We can estimate rapidly the quality of the measurements.

## THE SOFTWARE

The efficiency of the PC and its peripheries is mainly determined by the quality of the software. With the PC employed with the operating system CP/M the programme IRMA is written in the computer language Turbo Pascal. The software has to incorporate the following special conditions and functions in addition to the tasks of the testing facility:

-measurement of maximal 1,024 values per pixel
-storage of the measured values in one file per pixel this means that the file structure does not depend on the sensor type and the number of pixels per sensor
-each file is characterized by the so called housekeeping of the sensor and the measurement conditions
-handling with understandable service instructions on the computer screen
-guidance of the user through the programme by a menu
-the installation of new sensor types, new measuring and processing routines by the user

This conception was realised by the creation of 37 universally applicable software pieces which are used in eight programmes. In the structure of each piece we took account of the defined software interfaces. The software documentation describes how the user can add his own software pieces for further extensions. The advantage of this kind of software structure is that the user has only to know the defined software interfaces and not the whole programme of about 10,000 programme lines.

Another possibility is the off line processing of the stored files on other perhaps more powerful computers. It is easy to use the programme IRMA. The main menu (shown in figure 3) reflects the principal tasks of the test facility:

-the control of the parameters
-the different kinds of measurements
-the processing of the data
-the storing and the display of the results.

If an active key is pressed, one will see the next page of a submenu with further choices etc.

## CONCLUDING REMARKS

This paper has described briefly the IRMA-system, a processing system for testing of IR-sensors. By the help of IRMA we were able to qualify the method of the tests. The DC-measurements used, the so called broad-band-method, has demonstrated its suitability. The results on the responsivity and the noise equivalent power spectrum, are comparable with those determined by AC-measurements, that is the narrow-band-method. With these DC-measurements we obtain the entire continous spectrum which contracts with the results of AC-measurement, where only the values for few frequency-points are obtained. The DC-spectra begin, for all practical purposes, at 0 Hz. This allows us to estimate the 1/f-noise, the flicker-noise-part of the spectrum. And

this whole spectrum is obtained in a short period of time. That is because the DC-method allows us to automate the process of IR-sensor testing. These measurements of the IR-characteristics can be analysed statistically.

The broad band measuring method allows the measurement of infrared sensors independent of the read out principle. But it leads to problems in connection with offset, noise and drift of the sensor output signal.

The offset is caused by the background and surrounding temperature. Using the broad band method it is eliminated by measurements of the irradiated and the unirradiated sensor. The deviation in the moment of the shutter movement is calculated from this.

Modifications of IRMA have demonstrated in practice the flexibility of the hardware and the operating software. 1 1/2 years of use have shown that such a computer aided test facility like IRMA is a useful research tool to qualify IR-sensors for future applications in camera-systems on cosmic satellites.

*The hardware structure of IRMA*

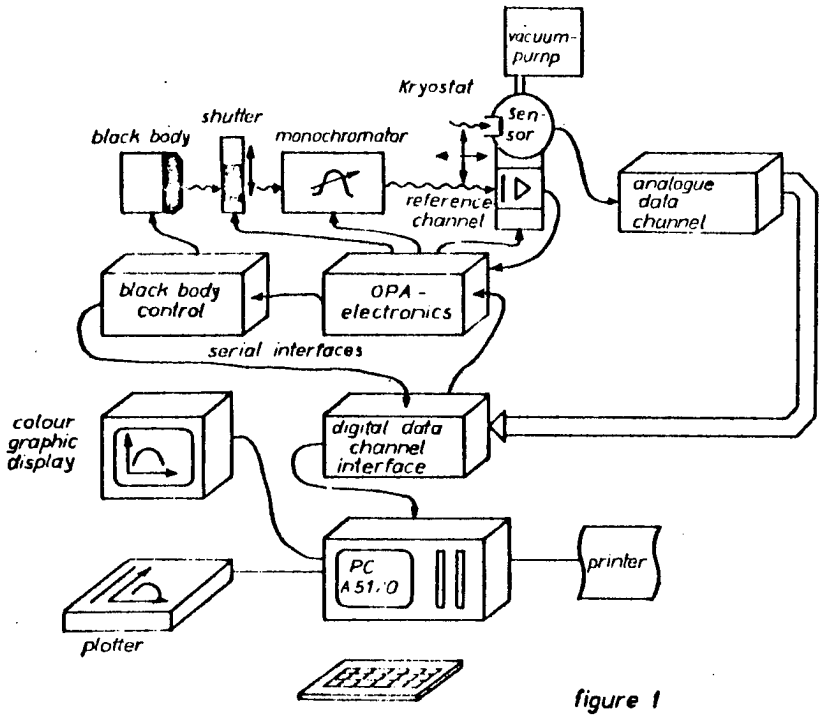


*figure 1*

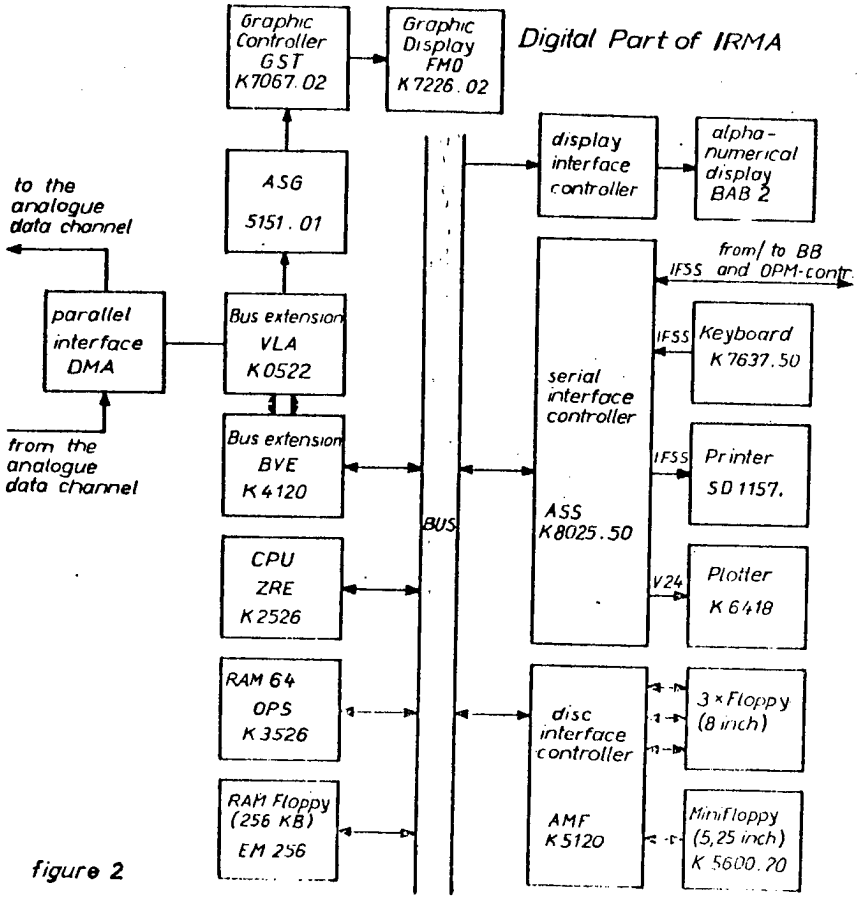
Digital Part of IRMA
Graphic Controller GST K7067.02
Graphic Display FMO K7226.02
ASG 5151.01
Bus extension VLA K0522
Bus extension BVE K4120
CPU ZRE K2526
RAM 64 OPS K3526
RAM Floppy (256 KB) EM 256
BUS
to the analogue data channel
parallel interface DMA
from the analogue data channel
display interface controller
alpha-numerical display BAB 2
from/to BB IFSS and OPM-contr.
serial interface controller
ASS K8025.50
IFSS
Keyboard K7637.50
IFSS
Printer SD1157.
V24
Plotter K6418
disc interface controller
AMF K5120
3 x Floppy (8 inch)
MiniFloppy (5,25 inch) K5600.20

figure 2

Software structure of IRMA

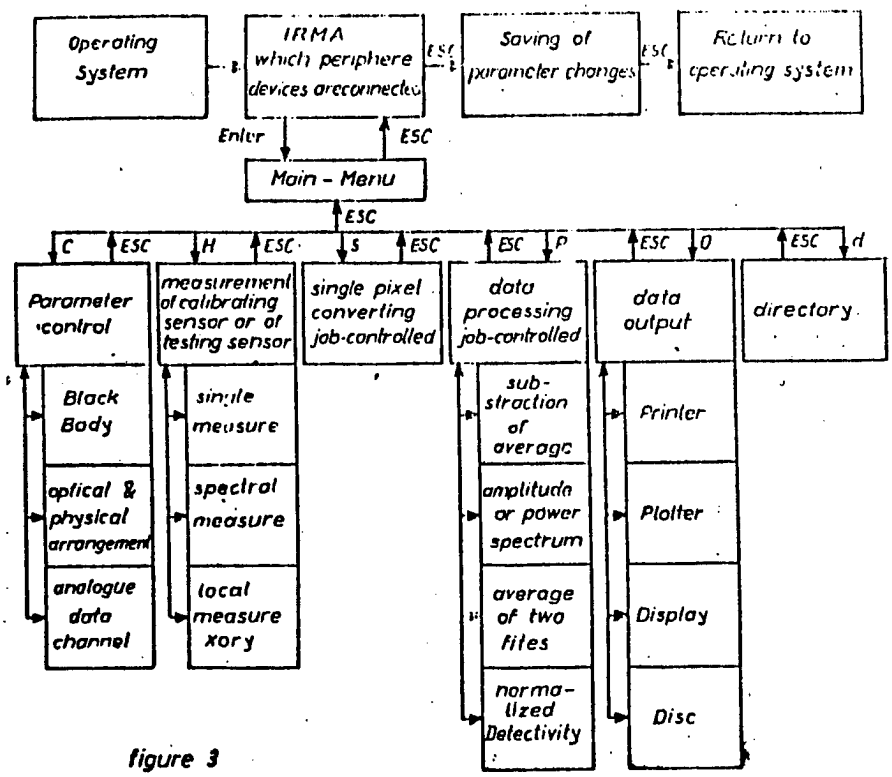


figure 3

# CABLE-FAULT TOLERANT LAN

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To improve the reliability of a LAN system a cable-fault tolerant arrangement was developed. Two independent LAN bus cables are used and the normal LAN stations are connected to the two buses via low cost arbiter units. The arbiter units are transparent and therefore no changes are needed in the LAN stations.

## INTRODUCTION

In industrial applications highly reliable systems are often required. At such an application our design team was facing the problem to improve the reliability of the HNS local area network system successfully used in other applications. Primary design goals were minimal added cost and the use of the proved LAN hardware and software units with minimal modification.

The HNS network [1] is of bus topology and uses CSMA/CD network access method according to the IEEE 802.3 standard [3]. The data transmission media is a 75 Ohm coax cable.

Analysing the probability and effect of different types of faults we have obtained the result that the LAN cable (transmit media) is the most critical part of the system and for the required high availability the LAN should be designed cable-fault tolerant.

In a bus structured LAN, if some of the stations (node units) fail the LAN may remain operating (with limited functionality). In the case of a fault on the bus lines the LAN breaks down. Moreover, in industrial plants the cables may be very vulnerable, at the damage and repair of other equipment the unintentional harm of the LAN cable has to taken in account.

Soft data transmission errors (e.g. errors caused by noise, EMP) are automatically detected by the LAN protocol and corrected by retransmission. However hard errors, such as permanent short circuits or a broken cable, can not be overcome by retransmission.

## REDUNDANCY SCHEMES

Faults causing hard errors are tolerable if redundancy is used. Redundancy may be used on several ways to make the system fault tolerant [2]. A well known static redundancy method is the 'triple modular redundancy'. This is a very costly method because the modules should be triplicated and voting units are also needed.

By the use of error detecting coding - which is a common practice in local area networks as frame check sequence or CRC - the faulty result can be masked out without voting module. By this way fault tolerance can be achieved only by duplicating the modules, in our case by duplicating the data transmission units. The LAN stations simultaneously transmit on both cables and the other stations are receiving simultaneously the messages on both cables. For proper operation all units of the transmit path and all units of the receive path (cable circuits, decoders, CRC checker) must be duplicated, reliable fault detection just at the cable receiver is not possible.

Searching for minimum cost solution the dynamic redundancy method was also investigated. A dynamic redundant system consists of several redundant modules, however with only one operating at a time. If a fault is detected in the operating module it is switched out and replaced by a spare one. This requires consecutive action of fault detection and fault recovery. Dynamic redundancy promised a little less redundant hardware in the LAN stations due to the

possibility of fault detection at the transmitting node. So our starting point at the design was the functional block diagram in Figure 1 according to the requirements of the dynamic redundancy scheme.

The switch module can be implemented in hardware or software as well. In the software implementation, to each LAN bus belongs an independent network interface unit connected to the station's system bus (e.g. two LAN interface cards are plugged into a PC motherboard). The software handles only one interface unit at a time, switch over is done by addressing the other interface unit.

For cost saving the switching should be done near the LAN cables, in this case less hardware must be duplicated. For this reason we have chosen hardware switching just before the tranceiver circuits. The tranceiver is recommended to be duplicated because some of the tranceiver faults (e.g. output short) have the same catastrophic impact on the LAN operation as the effect of a cable fault.

CABLE-FAULT DETECTION

The permanent cable faults can be detected on different ways.

- If consecutive retransmission trials are unsuccessful it can be assumed that a permanent cable fault has occurred. Using this method the data link layer of the software should be altered; a fault detection module and a 'switch to the spare unit' module should be added.

- Special built in hardware cable test unit can be added to the interface. This unit can use the TDR (time domain reflectometry) method in the intermessage gaps or on a frequency band differing from the frequency band of the data transfer.

- Shorts or cuts cause reflections. At tranceivers of the HNS LAN and most of the other CSMA/CD LANs the unwanted reflections cause the same symptom as the collision does: cable faults are detected as collisions. Many consecutive collisions indicate the probability of cable fault.

After analysing the trade-offs, we selected the latter fault detection method. Based on it we developed a so called arbiter unit which detects the probability of cable fault and automatically switches over to the other LAN cable (Fig 2). Every LAN station is connected through its own arbiter to the LAN cables. So not only the medium access control but also the fault detection and recovery control is distributed

in the system. A failed or switched-off station does not block the operation of the remaining part of the system.

THE ARBITER UNIT

The arbiter unit works as follows. At each collision a counter is incremented. A collision-free message transmission resets the counter. If the counter reaches the value of $n$, that is $n$ consecutive message collision symptoms have been observed, the transmission is switched over to the other cable. The switch over also resets the counter.

The receiver circuits of the two cables are always active and the receiver outputs are OR-ed together. This is necessary because the receiving stations do not know on which cable the transmitting node sends.

At the start of the operation each LAN station transmits or tries to transmit on the cable determined by the arbiter's default position.

At low data traffic the arbiters do not change the cable but during traffic jams some of the arbiters switch to the other cable because of the many collisions. Supposing that the stations send randomly and long time has elapsed from the start up the probability of the message distribution between cables tends to be equal. The value of $n$ has no influence on the data transmission properties.

If one of the cables is faulty then the transmitting stations are switching over from the faulty to the intact cable. For quick switch over a small $n$ is desired. However if $n$ is too small then at a high data traffic rate the arbiter tries often to transmit on the faulty cable because the number of collisions quickly surpasses $n$. The transmit trials on the faulty cable distort the back-off algorithm of the medium access. At the field use we set $n$=5 as a result of simulations and of data traffic considerations.

Summarizing the features of the method developed to make a LAN cable-fault tolerant with minimal added cost:

- beside of duplicating the cable and the tranceivers it needs only relatively simple arbiter units,
- the fault detection and recovery control is also distributed in the system, a failed or switched-off station does not stop the remaining part of the system,
- the arbiter units are fully transparent for the data transmission, no software modification is needed.

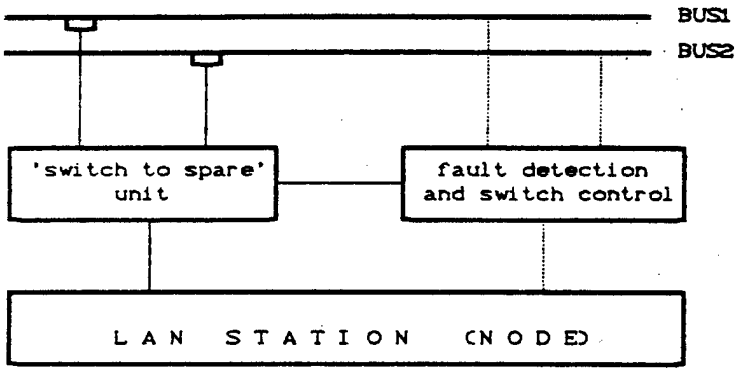


Fig. 1 Dynamic redundancy scheme

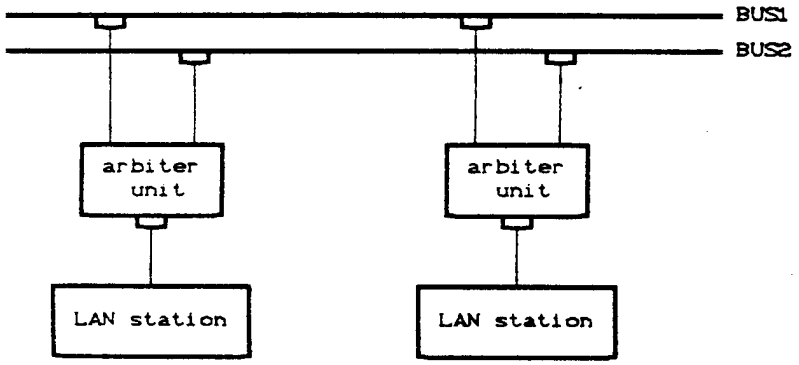


Fig. 2 Cable-fault tolerant LAN

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- END -

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